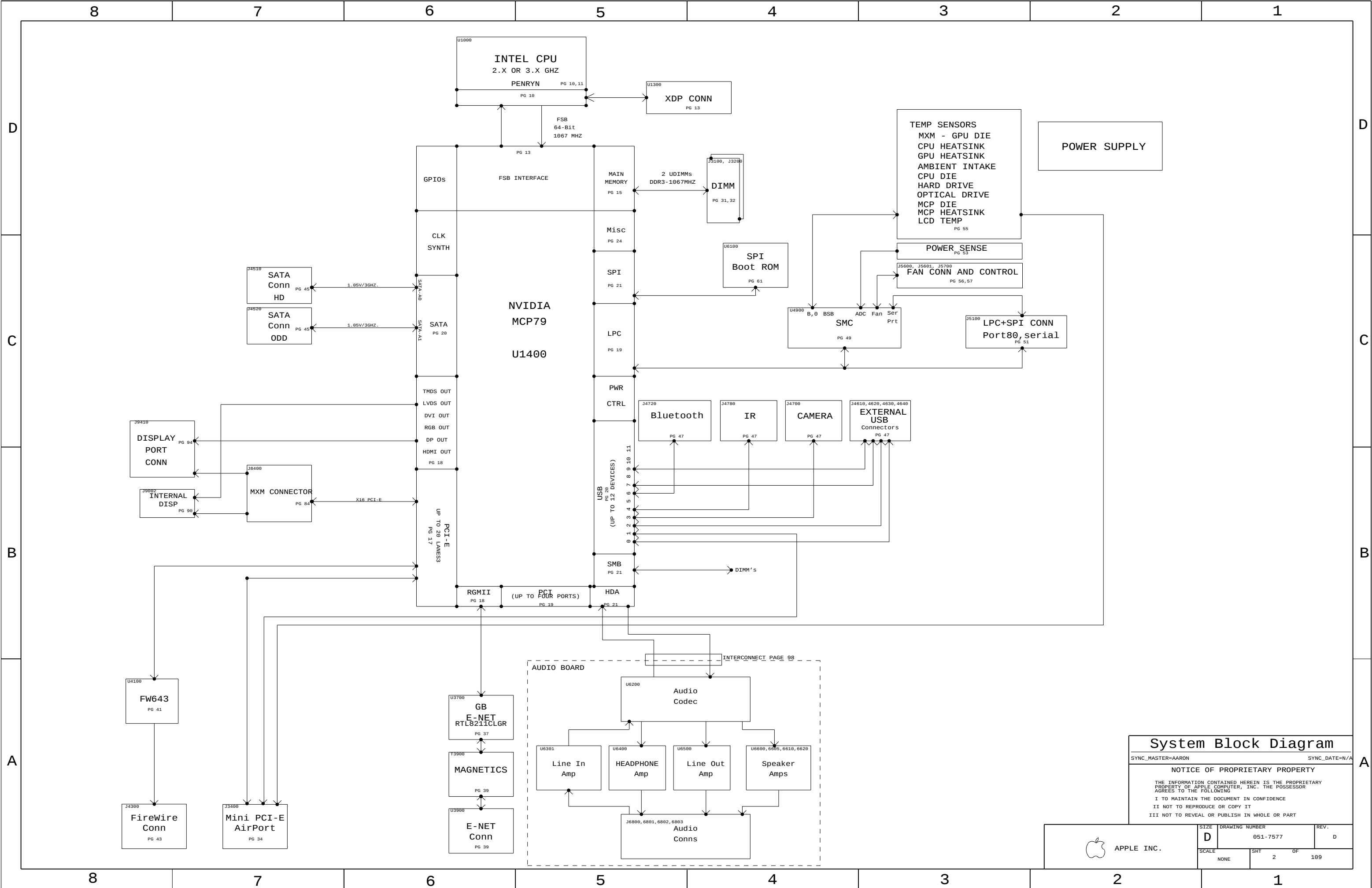


8		7		6		5		4		3		2		1													
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE										
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.												D		663445	PRODUCTION RELEASED	01/12/09	?										
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.																											
GINSU (K50)																											
REFERENCE FROM T18																											
LAST_MODIFIED=Fri Jan 9 17:28:50 2009																											
Page		Contents										Sync		Page		Contents										Sync	
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2		System Block Diagram										AARON		47		Thermal Sensors										DEREK	
3		Power Block Diagram										AARON		48		HD AND OD FAN										AARON	
4		BOM Configuration										AARON		49		CPU FAN										AARON	
5		Power Conn / Alias										K50_AARON		50		SPI ROM										AARON	
6		Functional / ICT Test										AARON		51		POWER SEQUENCING BLOCK DIAGRAM										MINGJING	
7		UNUSED SIGNAL ALIAS										K50_MASTER		52		PGOOD and Power Sequencing										K50	
8		SIGNAL & GND ALIASES										AARON		53		IMVP6 CPU VCore Regulator										K50	
9		CPU FSB										T18_MINGJING		54		IMVP6 3RD PHASE										K50	
10		CPU Power & Ground										T18_MINGJING		55		5V_S3 REGULATOR										K50	
11		CPU Decoupling & VID										MINGJING		56		MCP CORE REGULATOR										K50	
12		eXtended Debug Port (XDP)										SIJI		57		1.5V DDR SUPPLY										K50	
13		MCP CPU Interface										T18_MINGJING		58		1.05VS0/3.3V S5 SUPPLIES										K50	
14		MCP Memory Interface										T18_MINGJING		59		S3 & S0 FETs										K50	
15		MCP Memory Misc										T18_MINGJING		60		1V05 S5 POWER SUPPLY										K50	
16		MCP PCIe Interfaces										T18_MINGJING		61		1V8 POWER SUPPLY										K50	
17		MCP Ethernet & Graphics										T18_MINGJING		62		MXM PCIe, DP & Power										K50	
18		MCP PCI & LPC										T18_MINGJING		63		MXM I/O										K50	
19		MCP SATA & USB										T18_MINGJING		64		MXM PCIE CAPS										SIJI	
20		MCP HDA & MISC										T18_MINGJING		65		MXM ALIASES										SIJI	
21		MCP Power & Ground										T18_MINGJING		66		LVDS MUX RESISTORS										SIJI	
22		Debug: CPU										MINGJING		67		INTERNAL DISPLAY CONNS										SIJI	
23		MCP Standard Decoupling										MINGJING		68		DP MUX SUPPORT										SIJI	
24		MCP Graphics Support										SIJI		69		DISPLAYPORT SUPPORT										SIJI	
25		SB Misc										MINGJING		70		DisplayPort Connector										SIJI	
26		FSB/DDR3 Vref Margining										AARON		71		MLB: AUDIO CONNECTOR										DEREK	
27		MEMORY COUPLING CAPS										AARON		72		CPU/FSB Constraints										AARON	
28		DDR3 SO-DIMM Connector A										AARON		73		Memory Constraints										AARON	
29		DDR3 SO-DIMM CONNECTOR B										AARON		74		MCP Constraints 1										AARON	
30		DDR3 Support										T18_AARON		75		MCP Constraints 2										AARON	
31		PCI-E MiniCard Connector										AARON		76		Ethernet Constraints										AARON	
32		Ethernet PHY (RTL8211CL)										SIJI		77		FireWire Constraints										AARON	
33		Ethernet & AirPort Support										SIJI		78		SMC Constraints										AARON	
34		ETHERNET CONNECTOR										SIJI		79		GRAPHICS CONSTRAINTS										AARON	
35		FireWire LLC/PHY (FW643)										SIJI		80		K50/K51 SPECIFIC CONSTRAINTS										AARON	
36		FW: 1394B MISC										SIJI		81		K50/K51 RULE DEFINITIONS										AARON	
37		FIREWIRE CONNECTOR										SIJI															
38		SATA Connectors										SIJI															
39		EXTERNAL USB CONNECTORS										K50															
40		Internal USB Connections										AARON															
41		SMC										DEREK															
42		SMC Support										DEREK															
43		LPC+SPI Debug Connector										SIJI															
44		SMBUS CONNECTIONS										DEREK															
45		Current & Voltage Sensing										DEREK															
DRAWING																											
TITLE=K51																											
ABBREV=DRAWING																											
LAST_MODIFIED=Fri Jan 9 17:28:50 2009																											
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REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
D		663445	PRODUCTION RELEASED	01/12/09	?

LAST_MODIFIED=Fri Jan 9 17:28:50 2009

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55	73	5V_S3 REGULATOR	K50	08/19/2008
56	74	MCP CORE REGULATOR	K50	08/19/2008
57	75	1.5V DDR SUPPLY	K50	08/19/2008
58	76	1.05VS0/3.3V S5 SUPPLIES	K50	08/19/2008
59	78	S3 & S0 FETS	K50	08/19/2008
60	79	1V05 S5 POWER SUPPLY	K50	08/19/2008
61	80	1V8 POWER SUPPLY	K50	08/19/2008
62	84	MXM PCIe, DP & Power	K50	07/30/2008
63	85	MXM I/O	K50	07/30/2008
64	86	MXM PCIE CAPS	SIJI	09/11/2008
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66	89	LVDS MUX RESISTORS	SIJI	09/11/2008
67	90	INTERNAL DISPLAY CONNS	SIJI	09/11/2008
68	91	DP MUX SUPPORT	SIJI	09/11/2008
69	93	DISPLAYPORT SUPPORT	SIJI	09/11/2008
70	94	DisplayPort Connector	SIJI	09/11/2008
71	98	MLB: AUDIO CONNECTOR	DEREK	09/11/2008
72	100	CPU/FSB Constraints	AARON	03/27/2008
73	101	Memory Constraints	AARON	03/27/2008
74	102	MCP Constraints 1	AARON	03/27/2008
75	103	MCP Constraints 2	AARON	03/27/2008
76	104	Ethernet Constraints	AARON	03/27/2008
77	105	FireWire Constraints	AARON	03/27/2008
78	106	SMC Constraints	AARON	03/27/2008
79	107	GRAPHICS CONSTRAINTS	AARON	03/27/2008
80	108	K50/K51 SPECIFIC CONSTRAINTS	AARON	05/20/2008
81	109	K50/K51 RULE DEFINITIONS	AARON	05/20/2008



System Block Diagram

SYNC_MASTER=AARON SYNC_DATE=N/A

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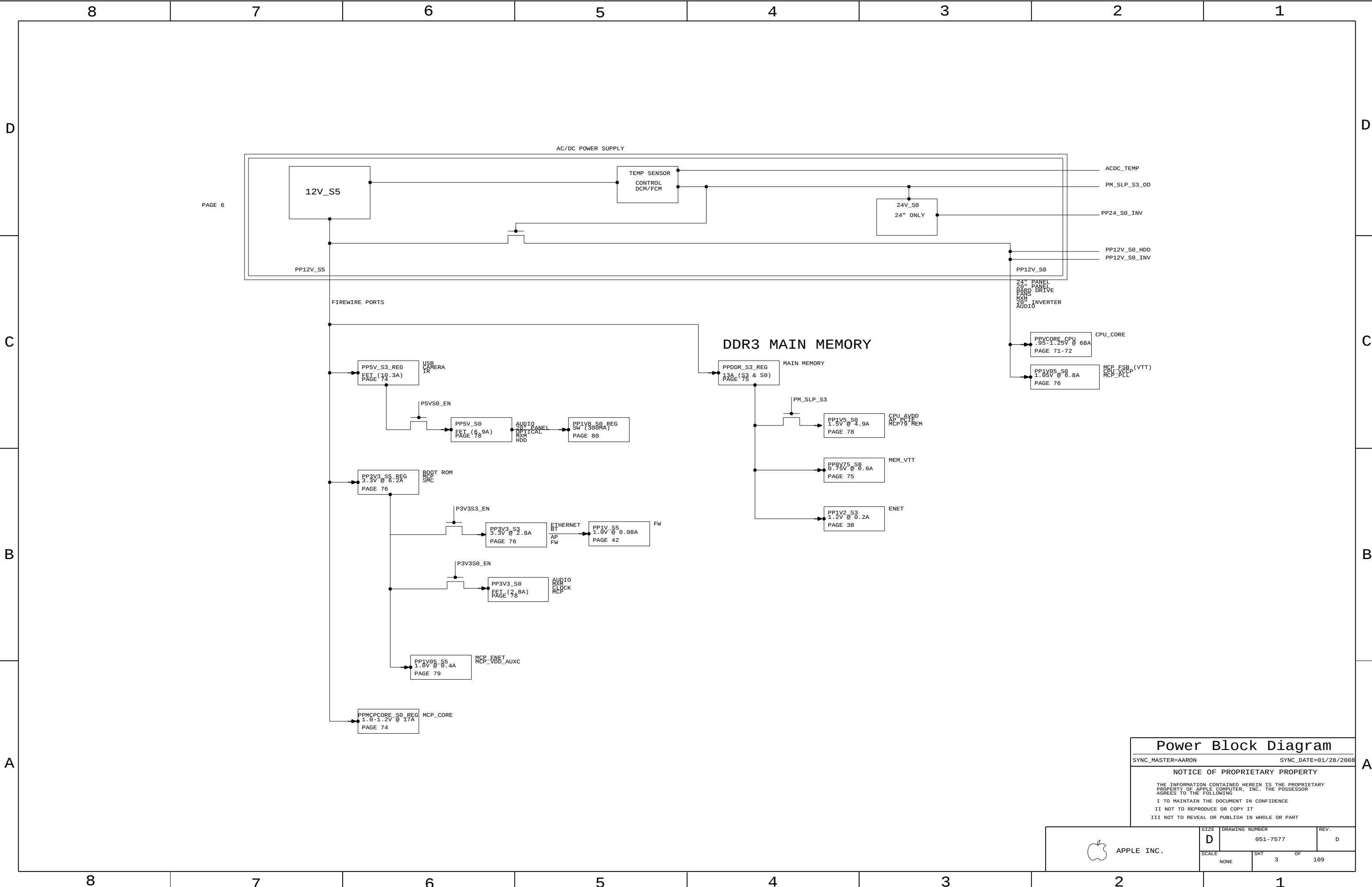
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Power Block Diagram

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NONE		3	109

BOM Variants

BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9501	PCBA, MLB, K50, GOOD	20_INCH_LCD, 2P66GHZ_CPU, BASIC, IG, RENESAS_FET
607-2695	K50 MLB DEVELOPMENT	DEVELOPMENT, XDP_CONN, LPCPLUS, VREFMRGN, MCP_PWR_SENSE

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9765	PCBA, MLB, K51, BETTER	24_INCH_LCD, 2P66GHZ_CPU, BASIC, IG, RENESAS_FET
630-9773	PCBA, MLB, K51, BEST	24_INCH_LCD, 2P93GHZ_CPU, BASIC, MXM, MXM_PWR_SENSE, 12V_PWR_SENSE, 24_INCH_MXM, RENESAS_FET
630-9774	PCBA, MLB, K51, CTO_ULT	24_INCH_LCD, 3P06GHZ_CPU, BASIC, MXM, MXM_PWR_SENSE, 12V_PWR_SENSE, 24_INCH_MXM, RENESAS_FET
607-4252	K51 MLB DEVELOPMENT	DEVELOPMENT, XDP_CONN, LPCPLUS, VREFMRGN, MCP_PWR_SENSE

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE, MCP_TDIODE, MCP79, CPUV_PHASE3, XDP, CPU_TDIODE, MCP_B02, PRODUCTION
MCP79	BOOT_MODE_USER, MEMRESET_HW, MEMRESET_MCP

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3705	1	IC, PRQ, PDC, SLGEB, 2.66, 55W, 1066, 6E, 6N, PGA	CPU	CRITICAL	2P66GHZ_CPU
337S3706	1	IC, PRQ, PDC, SLGEB, 2.93, 55W, 1066, 6E, 6N, PGA	CPU	CRITICAL	2P93GHZ_CPU
337S3707	1	IC, PRQ, PDC, SLGEA, 3.06, 55W, 1066, 6E, 6N, PGA	CPU	CRITICAL	3P06GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON (DELETED HDCP ROM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0636	1	IC_GMCP_MCP79-B02,35X35MM, BGA1437, DT	U1400	CRITICAL	MCP_B02
338S0654	1	IC_FW643-06,1394B, REV-E	U4100	CRITICAL	
820-2404	1	PCB, FAB, IO ALIGNMENT, K50/K51	I01	CRITICAL	
825-7122	1	MLB LABEL, 48.0X4.8	X14	CRITICAL	
341T0135	1	EFI ROM, K50/K51	U6100	CRITICAL	
511S0038	1	CONN, INTEL SKT-P, BGA, 26X26-479	U1000	CRITICAL	
338S0570	1	IC_RTL8211CL, GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	

K50 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7577	1	PCB, SCHEM, MLB, K50	SCH1		20_INCH_LCD
820-2347	1	PCB, FAB, MLB, K50, HF	MLB1		20_INCH_LCD
341T0132	1	IC, SMC, K50	U4900	CRITICAL	20_INCH_LCD
11450305	1	RES, 7.87K, 0402, 1%, 1/16W, LF	R7117		20_INCH_LCD
13250205	1	CAP, CER, 270PF, 10%, 50V, 0402	C7113		20_INCH_LCD
13250178	1	CAP, CER, 0.47UF, 10%, 6.3V, 0402	C7128		20_INCH_LCD
13250082	1	CAP, CER, 0.068UF, 10%, 10V, 0402	C7134		20_INCH_LCD

K51 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7840	1	PCB, SCHEM, MLB, K51	SCH1		24_INCH_LCD
820-2491	1	PCB, FAB, MLB, K51, HF	MLB1		24_INCH_LCD
341T0164	1	IC, SMC, K51	U4900	CRITICAL	24_INCH_LCD
11450308	1	RES, 0.45K, 0402, 1%, 1/16W, LF	R7117		24_INCH_LCD
13250010	1	CAP, CER, 390PF, 10%, 50V, 0402	C7113		24_INCH_LCD
13250178	1	CAP, CER, 0.47UF, 10%, 6.3V, 0402	C7128		24_INCH_LCD
13250082	1	CAP, CER, 0.068UF, 10%, 10V, 0402	C7134		24_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152-0104	152-0099		L7100, L7101, L7200	MSQ-1211-R36L-F
152-0105	152-0101		L7530	MSQ-1211-1R5L-F

BOM Configuration

SYNC_MASTER=AARON	SYNC_DATE=N/A
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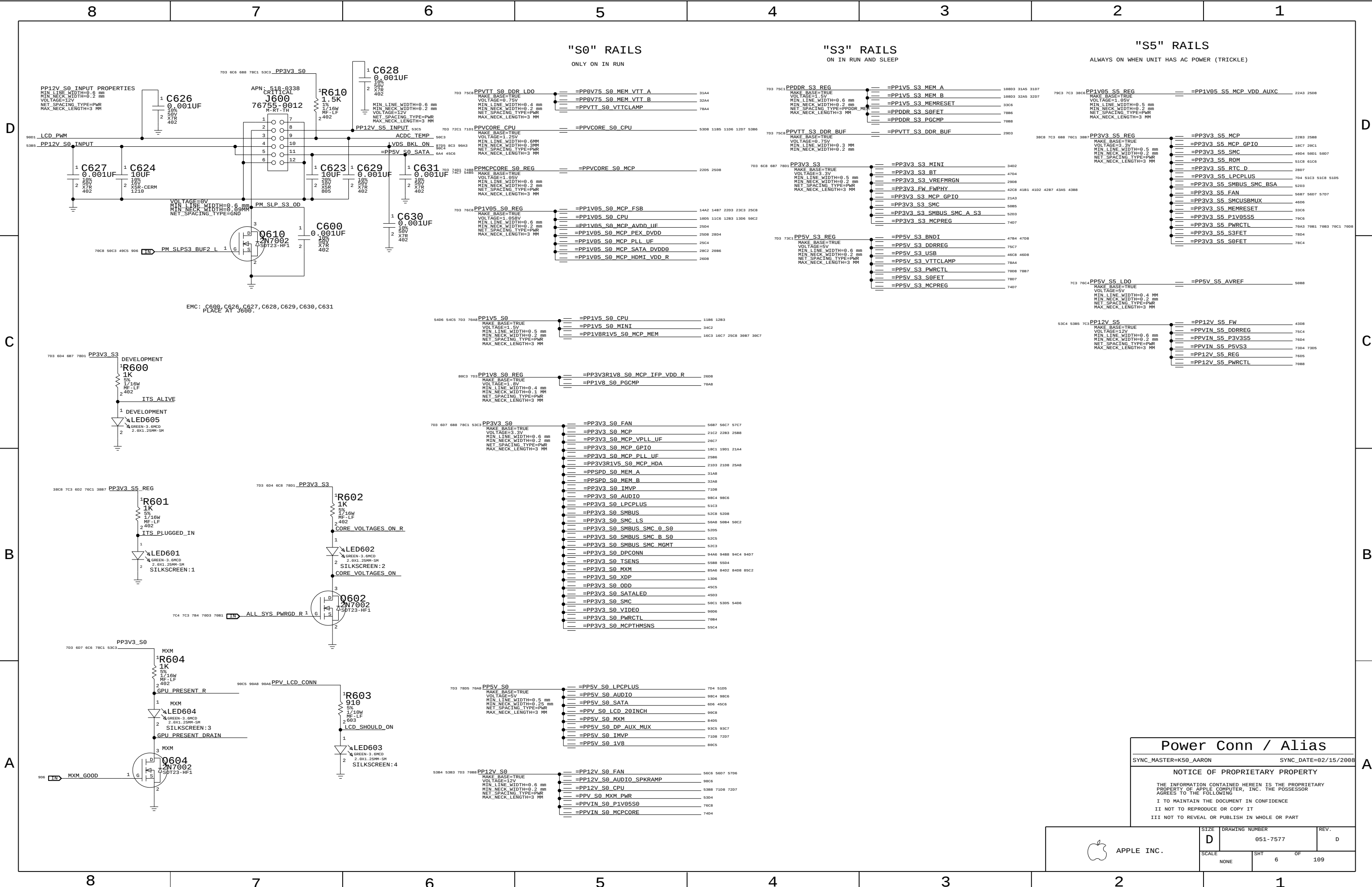
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Power Conn / Alias

SYNC_MASTER=K50_AARON

SYNC_DATE=02/15/2008

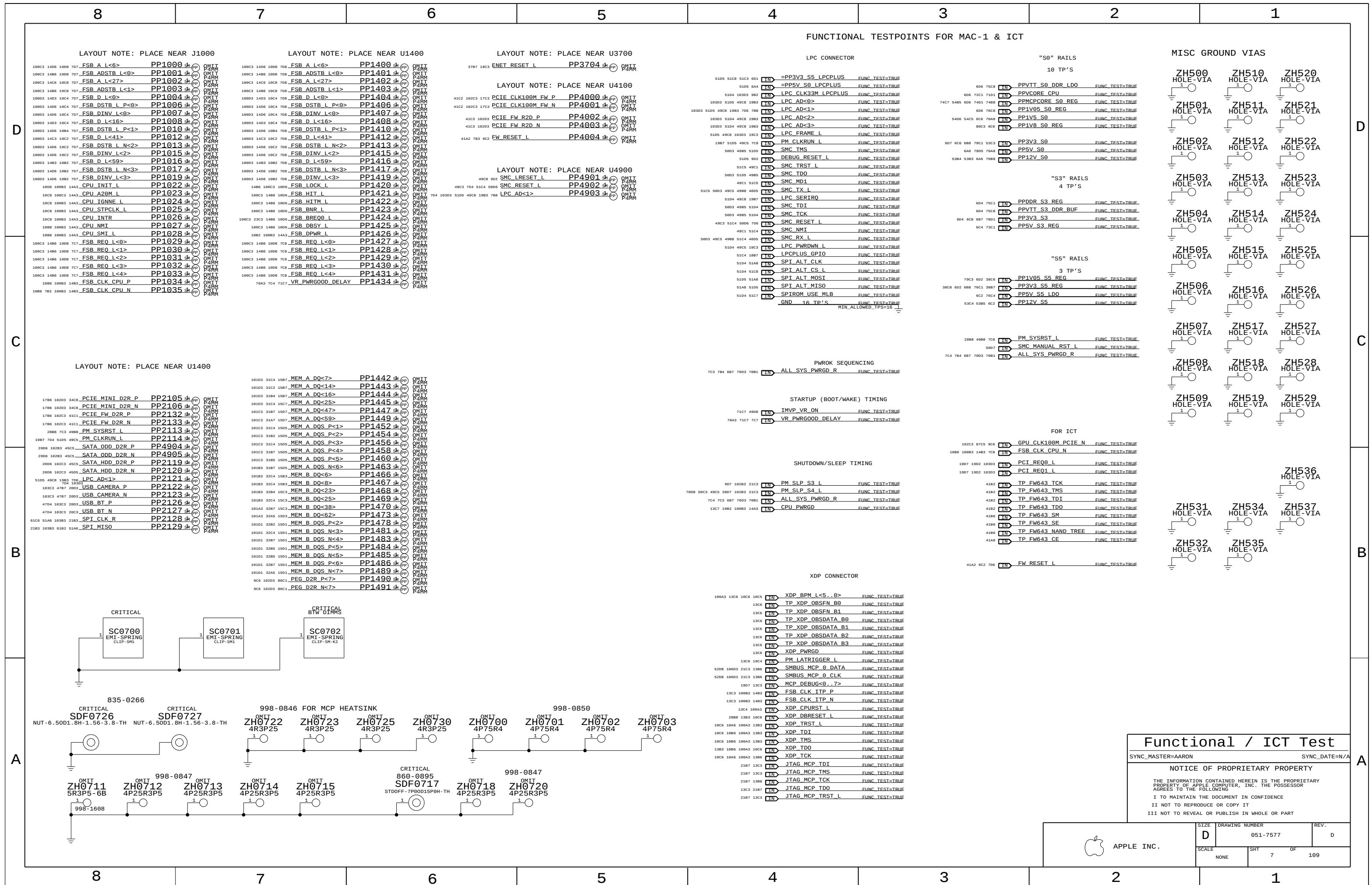
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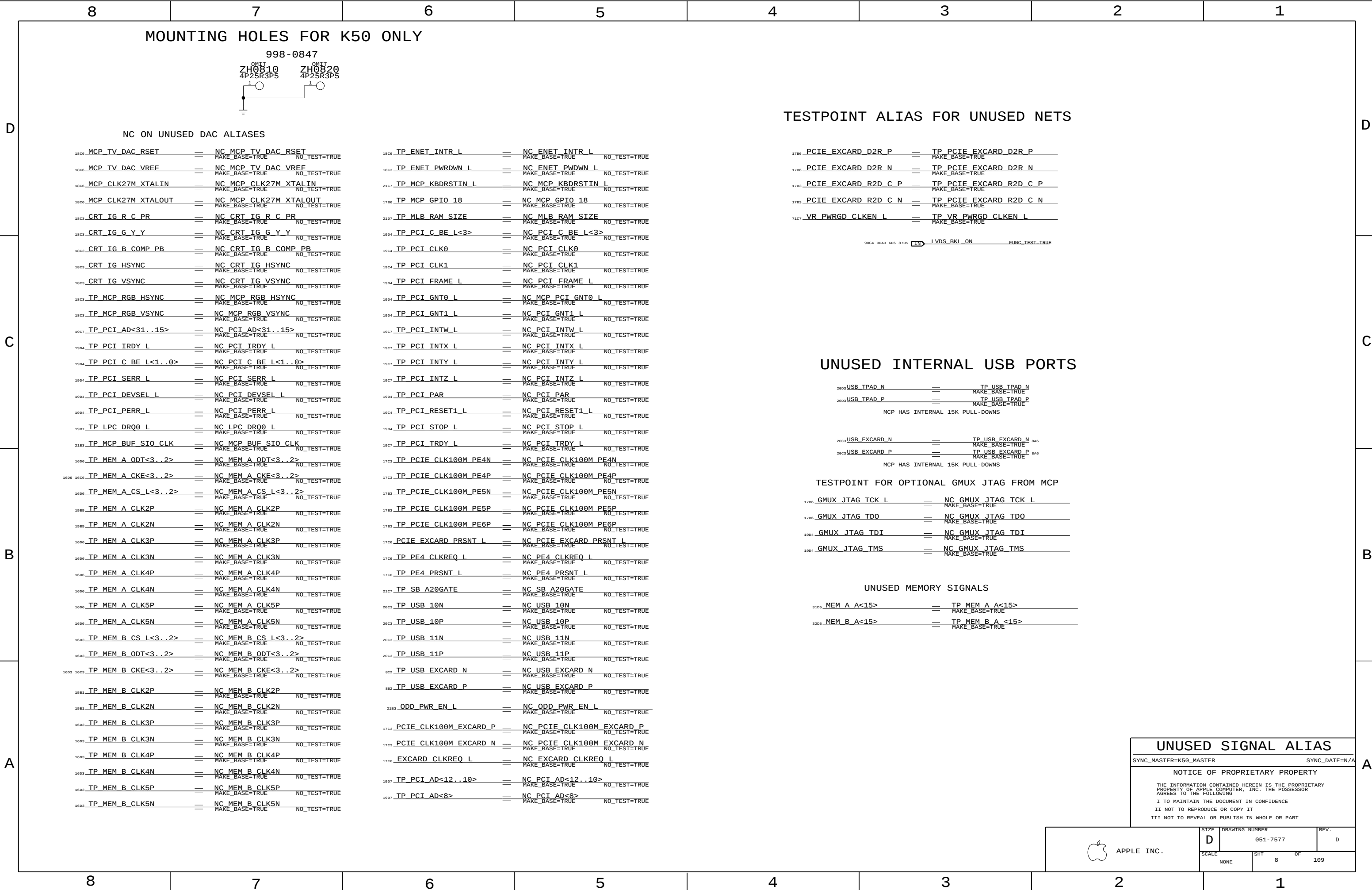
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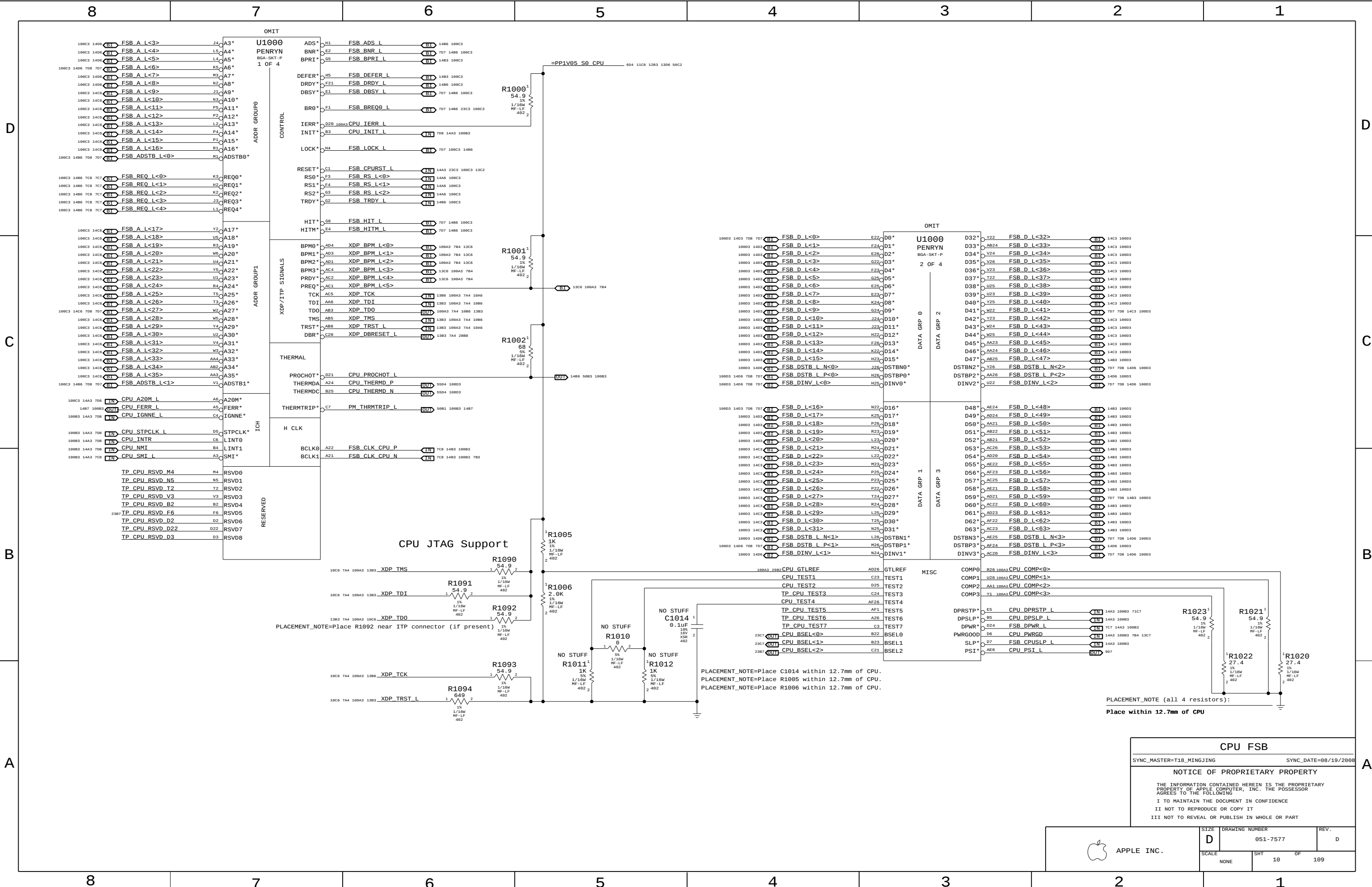
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CPU FSB

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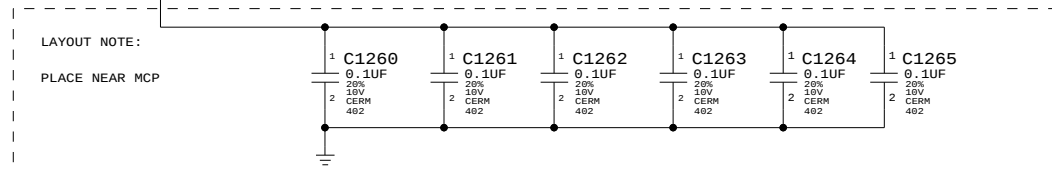
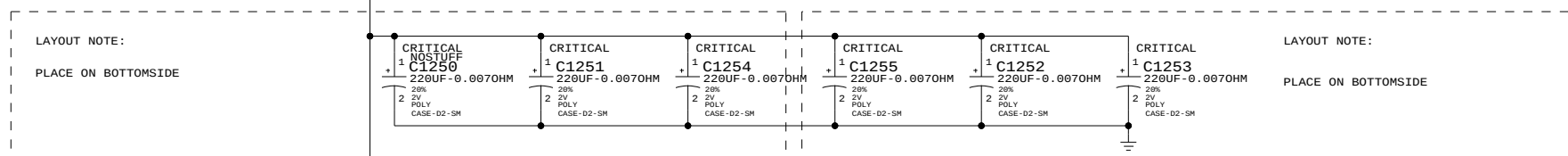
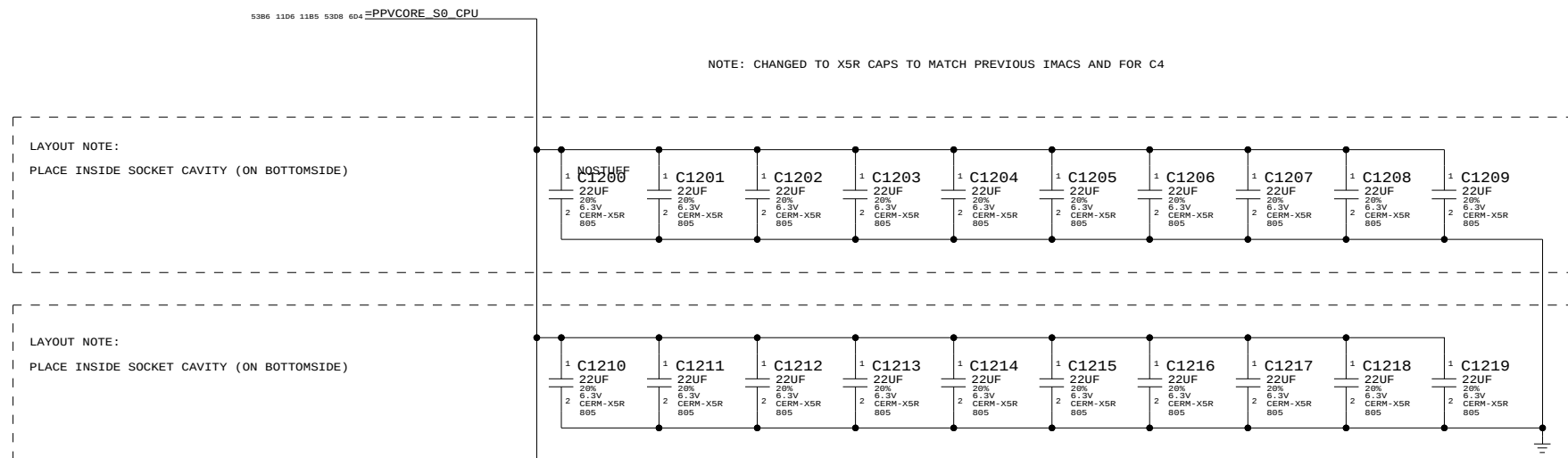
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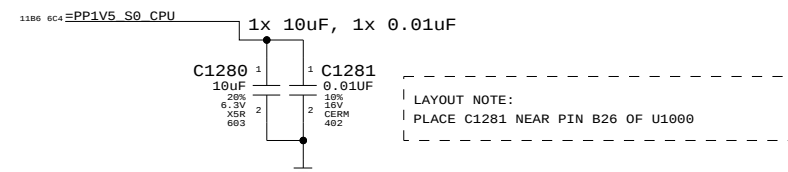
6X 220UF. 32X 22UF 0805



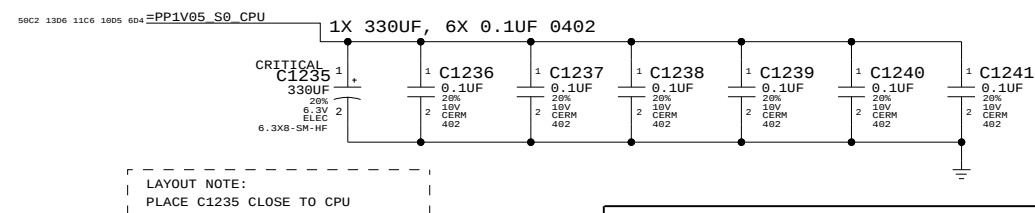
CPU VCORE VID CONNECTIONS



VCCA (CPU AVdd) DECOUPLING



VCCP (CPU I/O) DECOUPLING



CPU Decoupling & VID	
SYNC_MASTER=MINGJING	SYNC_DATE=08/19/2008
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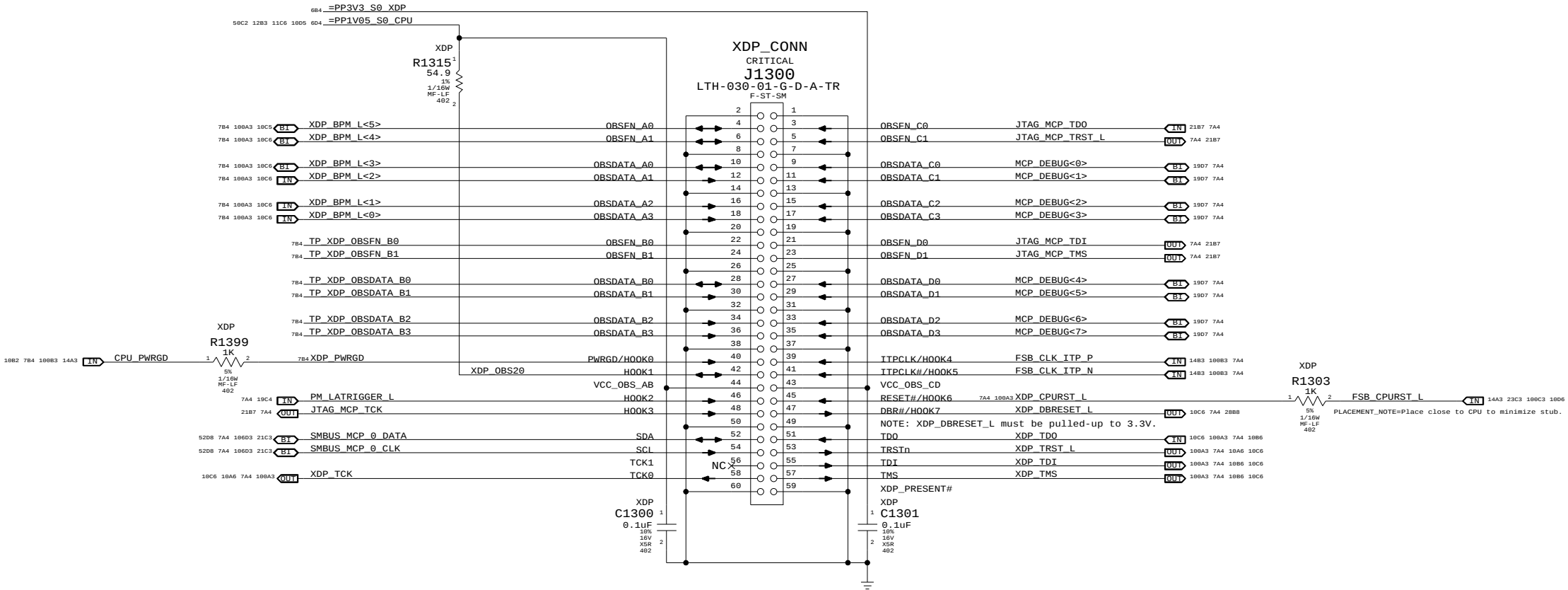
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MCP79-specific pinout



eXtended Debug Port (XDP)

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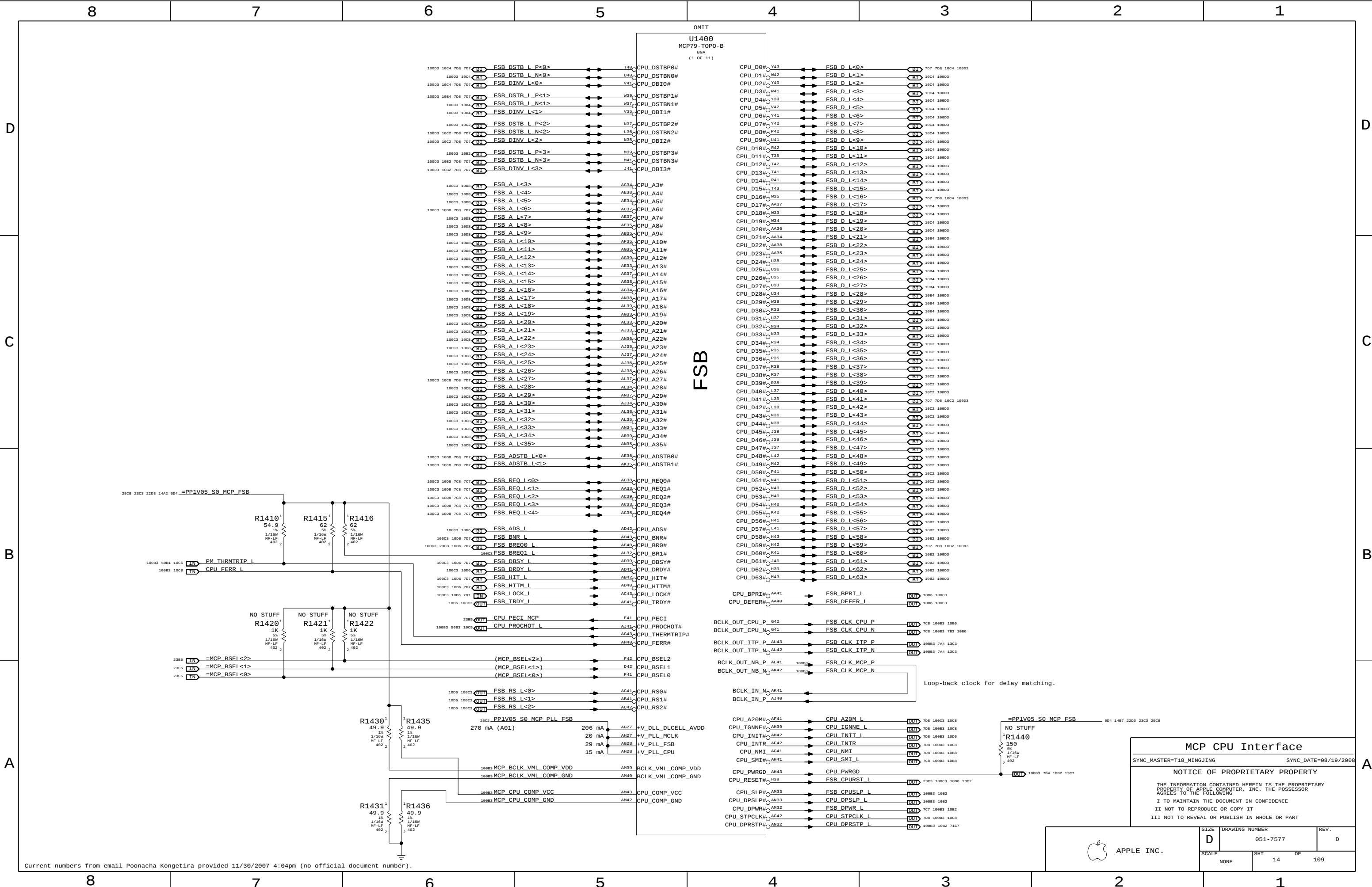
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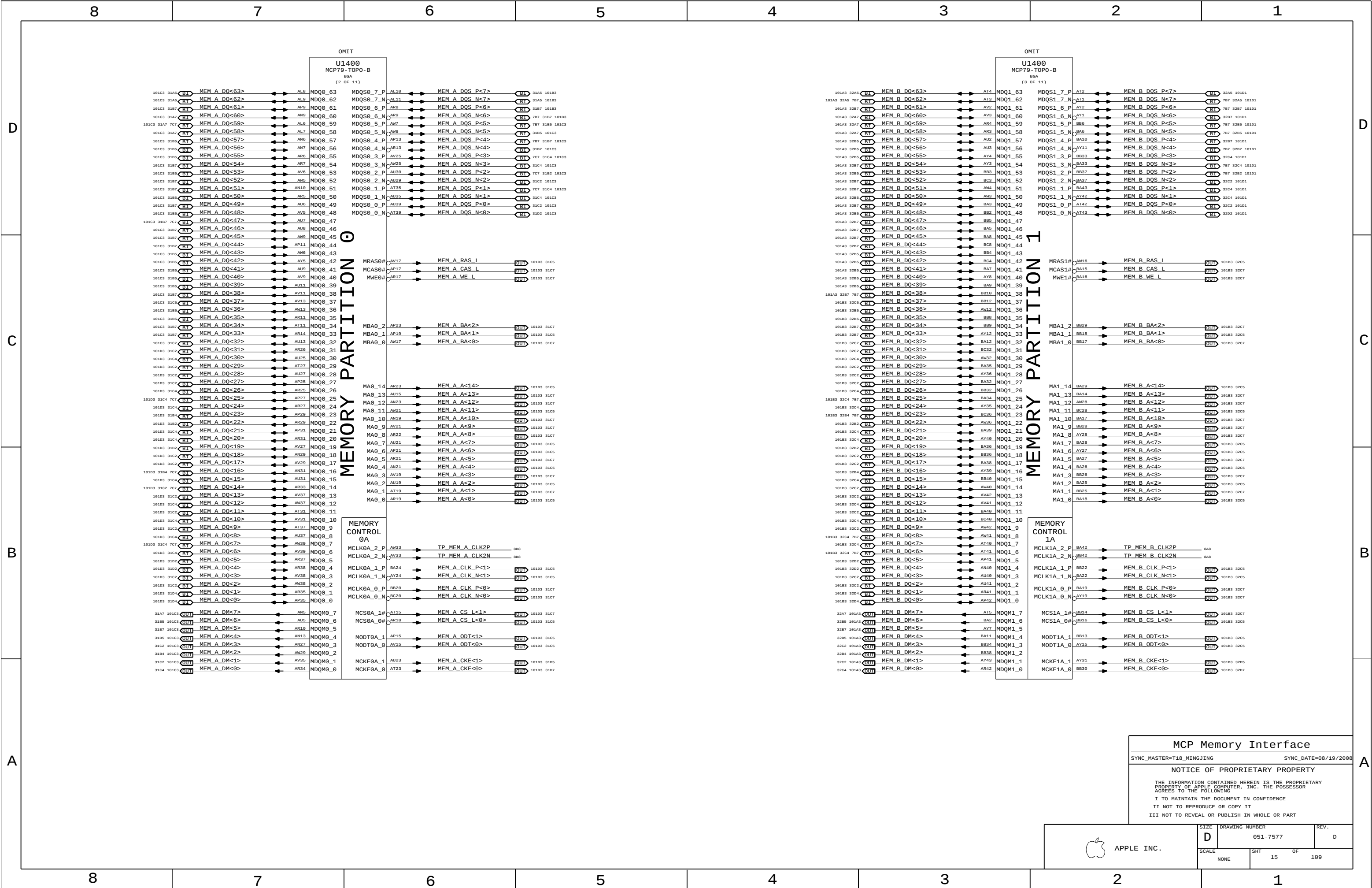


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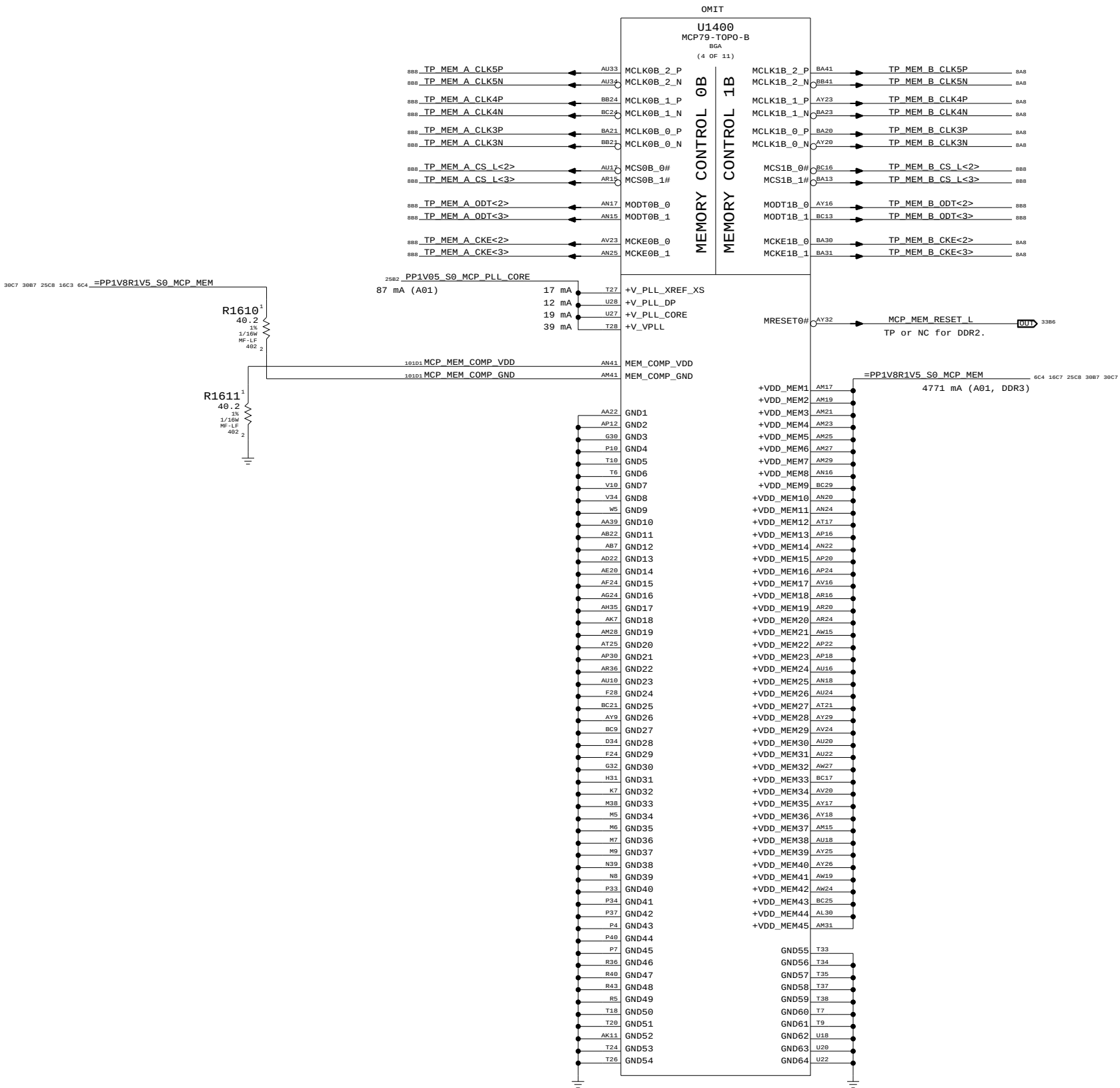
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MCP Memory Misc

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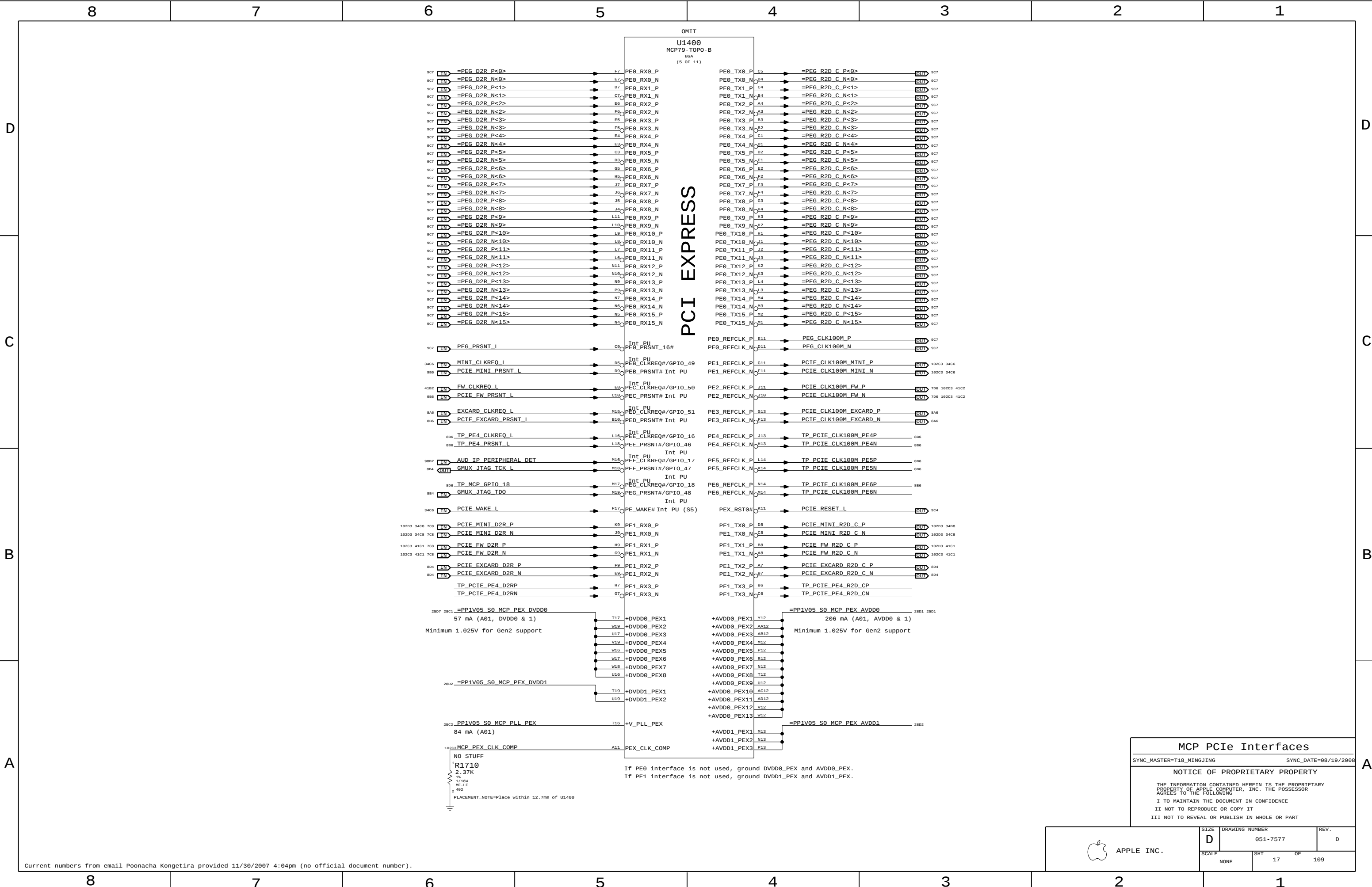
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NONE	16	109



MCP PCIe Interfaces

SYNC_MASTER=T18_MINGJING

SYNC_DATE=08/19/2008

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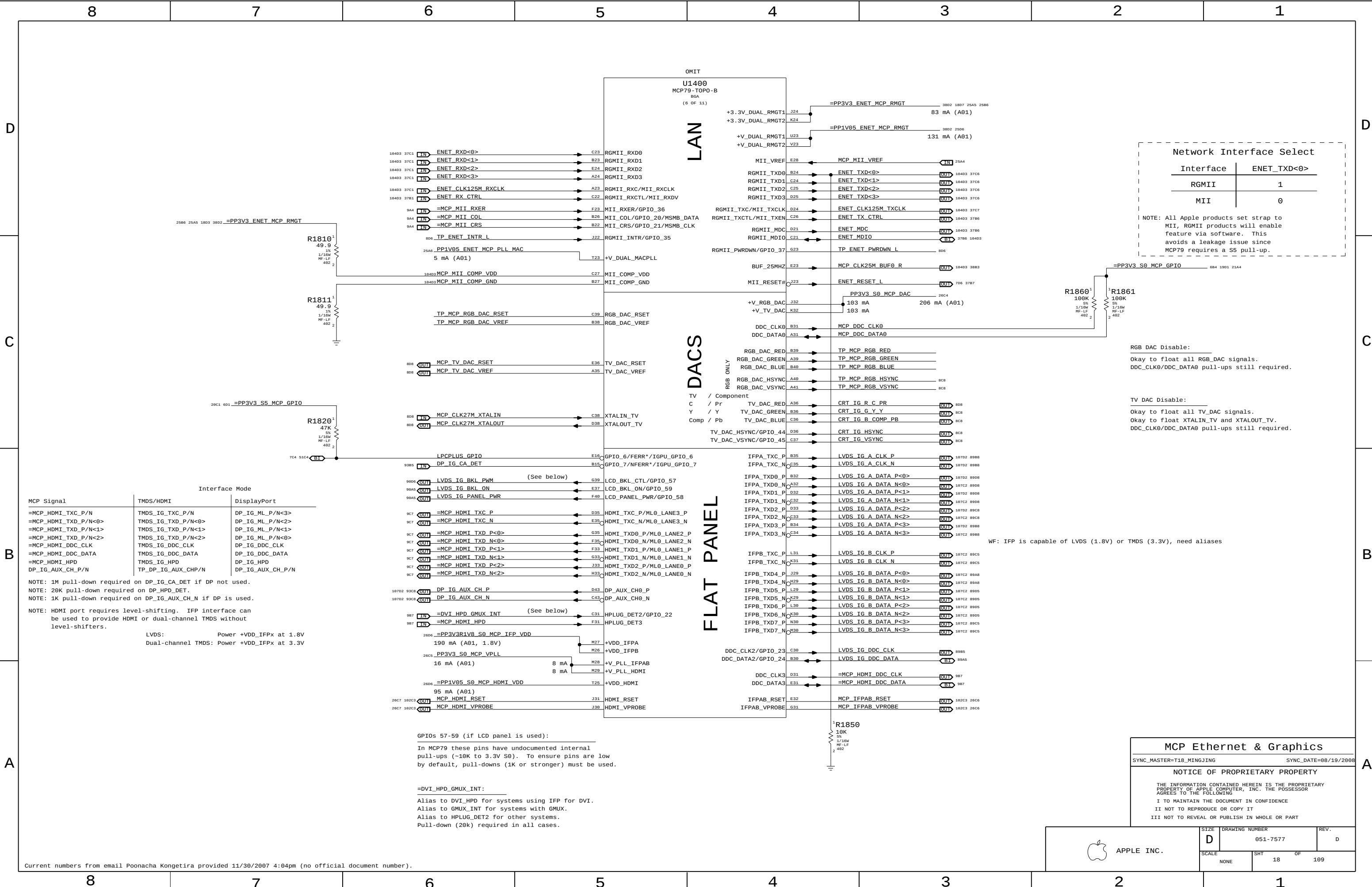
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NONE		17	109



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

MCP Signal	Interface Mode	
	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

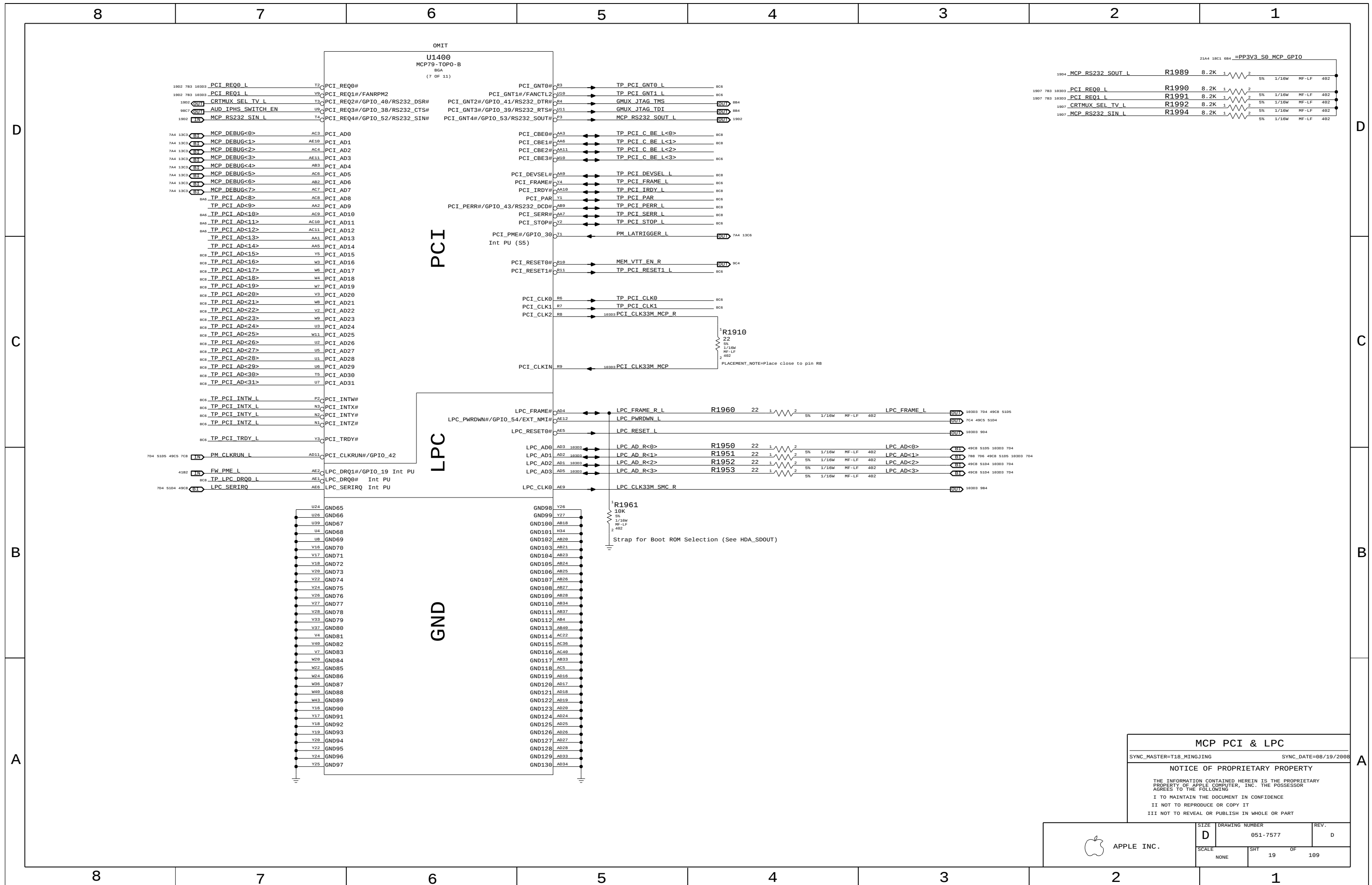
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

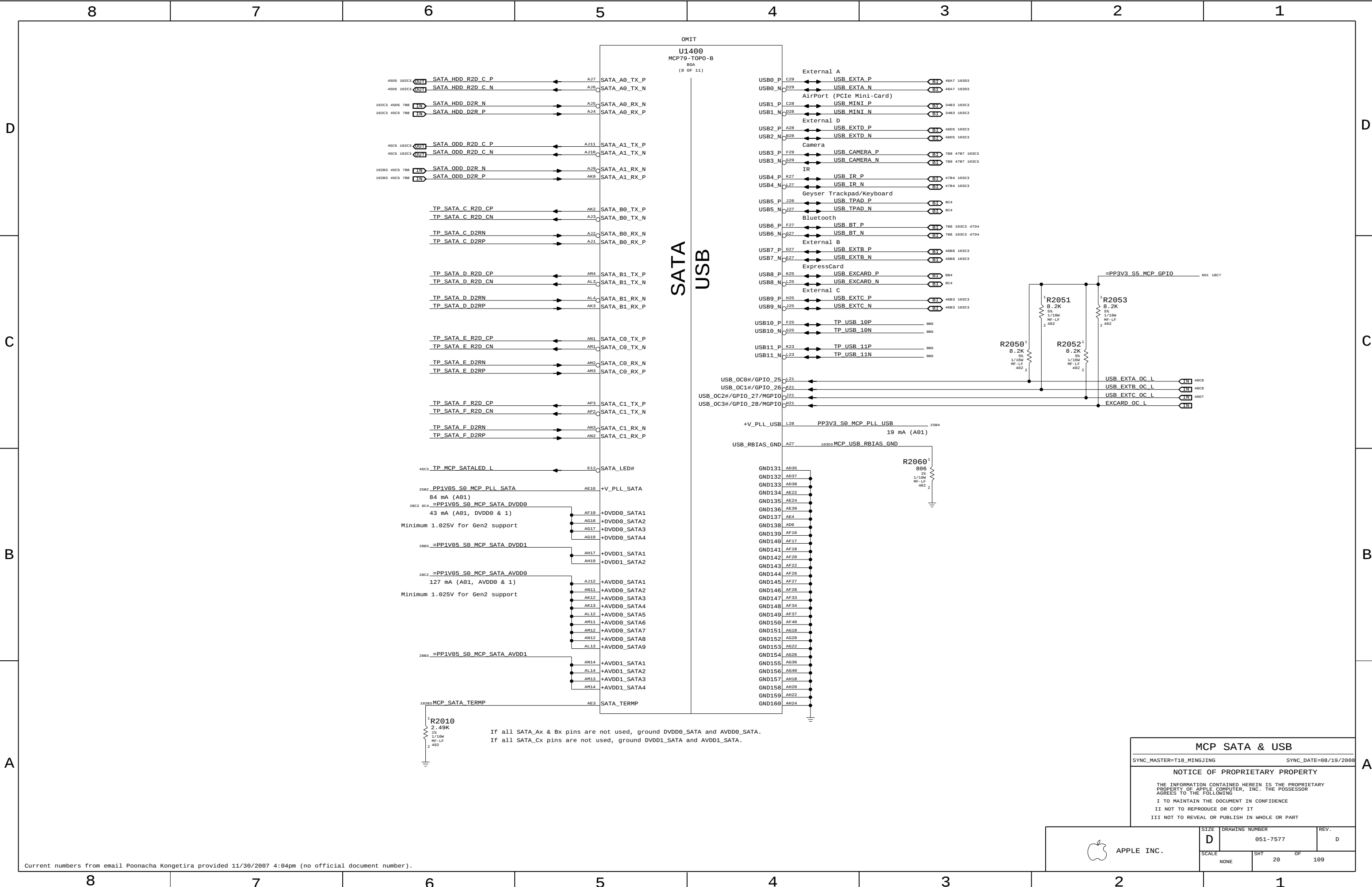
GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT: _____
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

 APPLE INC.

SIZE D	DRAWING NUMBER 051-7577	REV. D
SCALE NONE	SHT 18	OF 109





If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

SYNC_MASTER=T18_MINGJING SYNC_DATE=08/19/2008

NOTICE OF PROPRIETARY PROPERTY

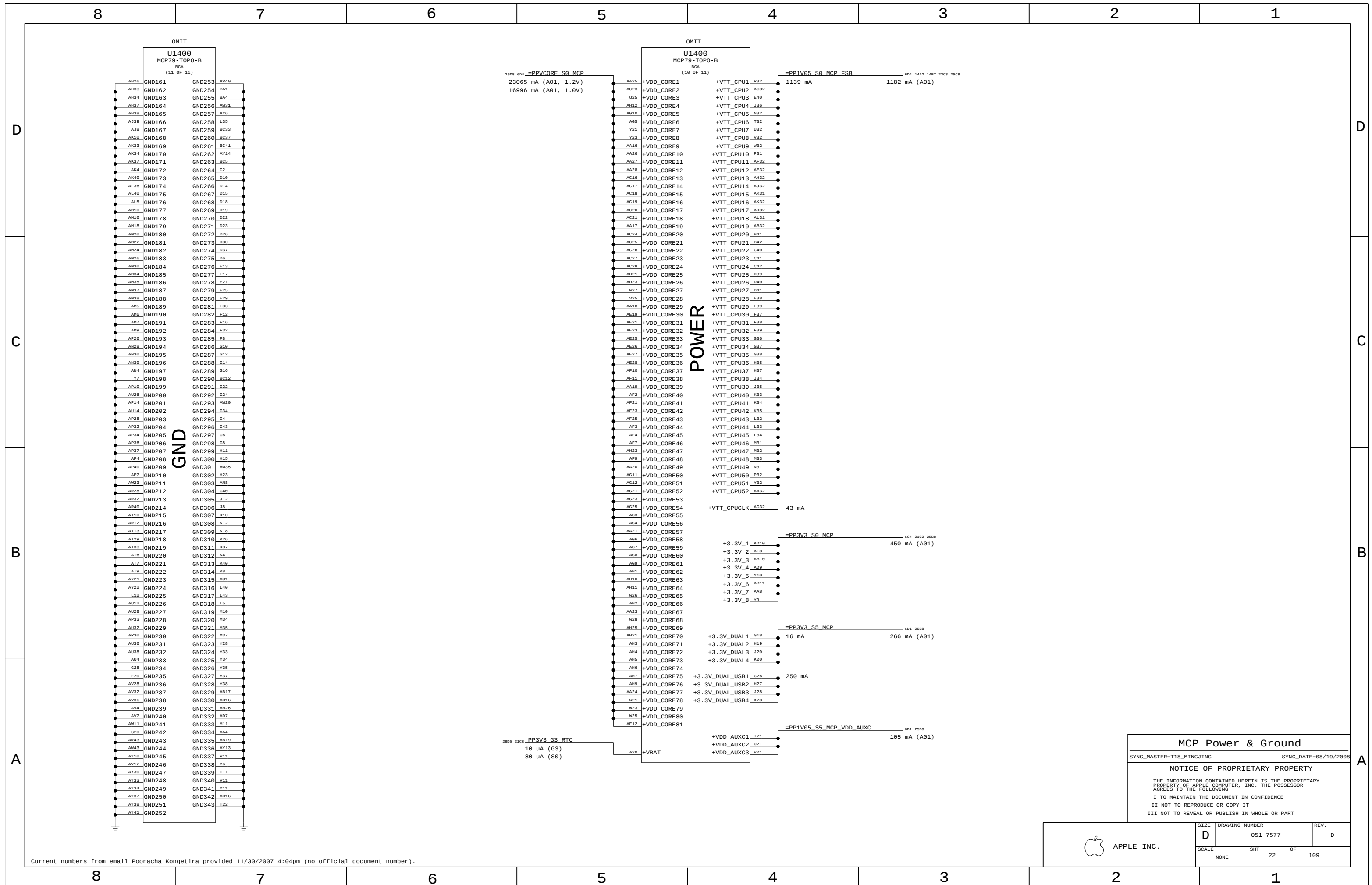
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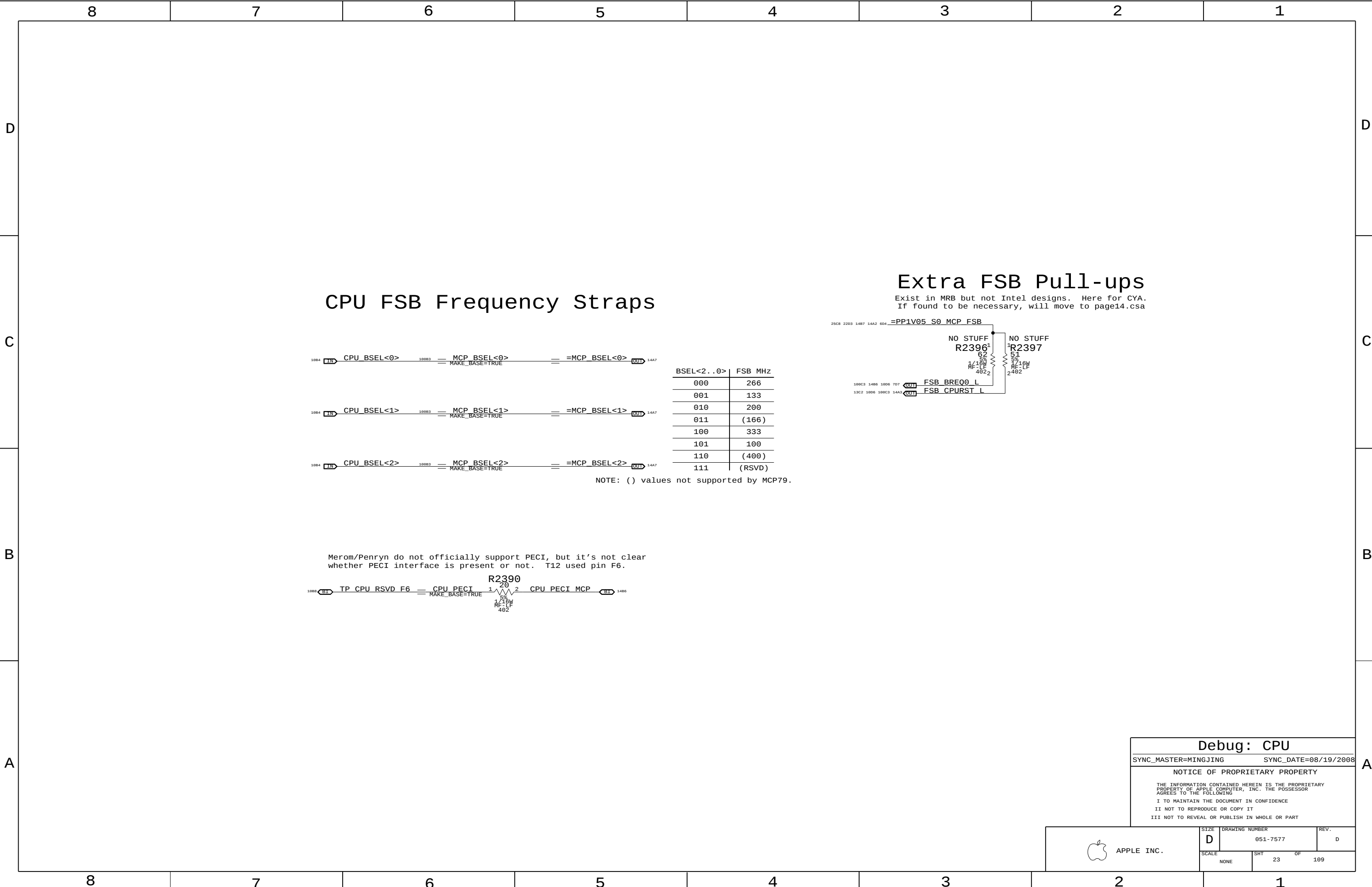
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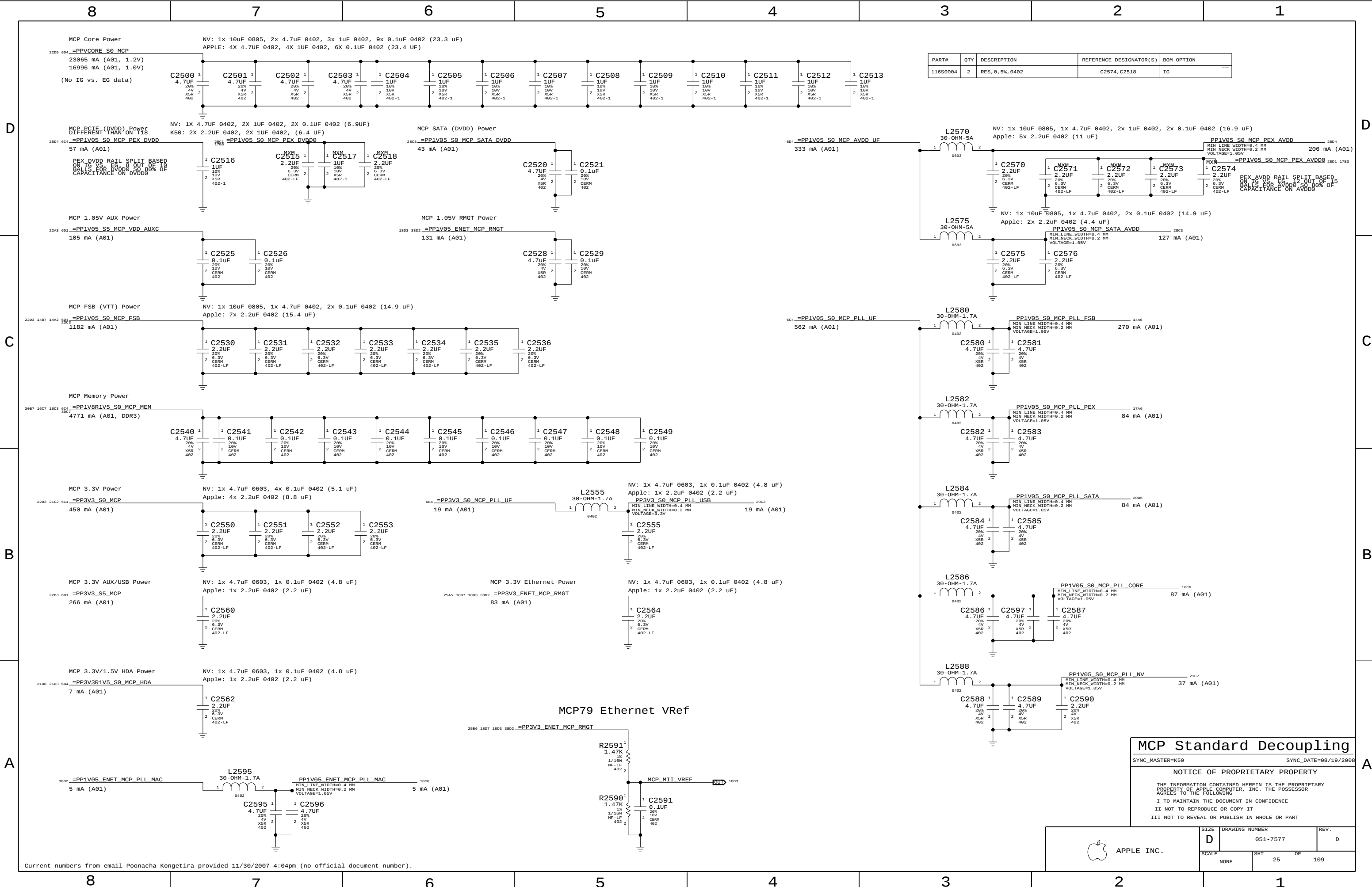
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

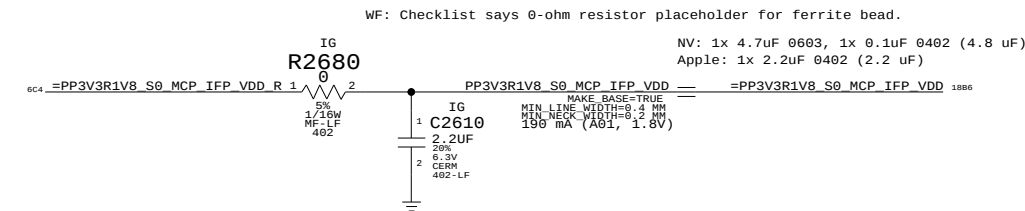
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7577	D
SCALE		SHT	OF
NONE		20	109



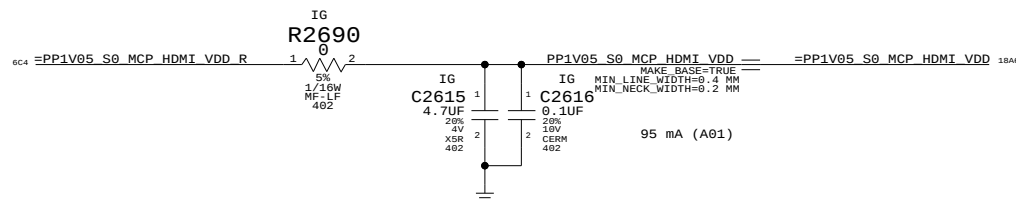




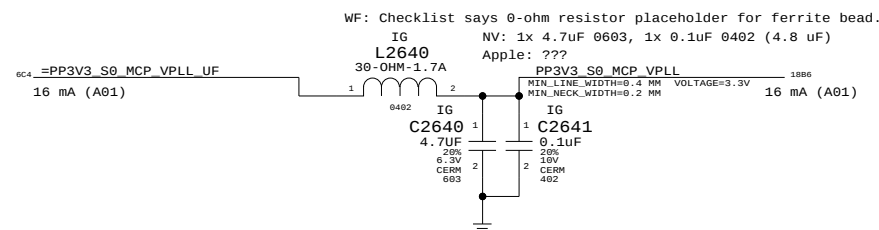
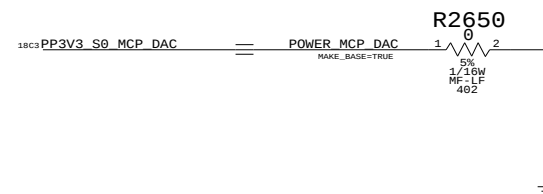
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



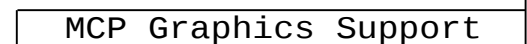
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES, 0, 5%, 402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES, 0, 5%, 402	C2616		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES, 0, 5%, 402	C2641		MXM



SYNC_MASTER=SIJI SYNC_DATE=09/11/2008

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SIZE D	DRAWING NUMBER 051-7577	REV. D
SCALE NONE	SHT 26	OF 109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

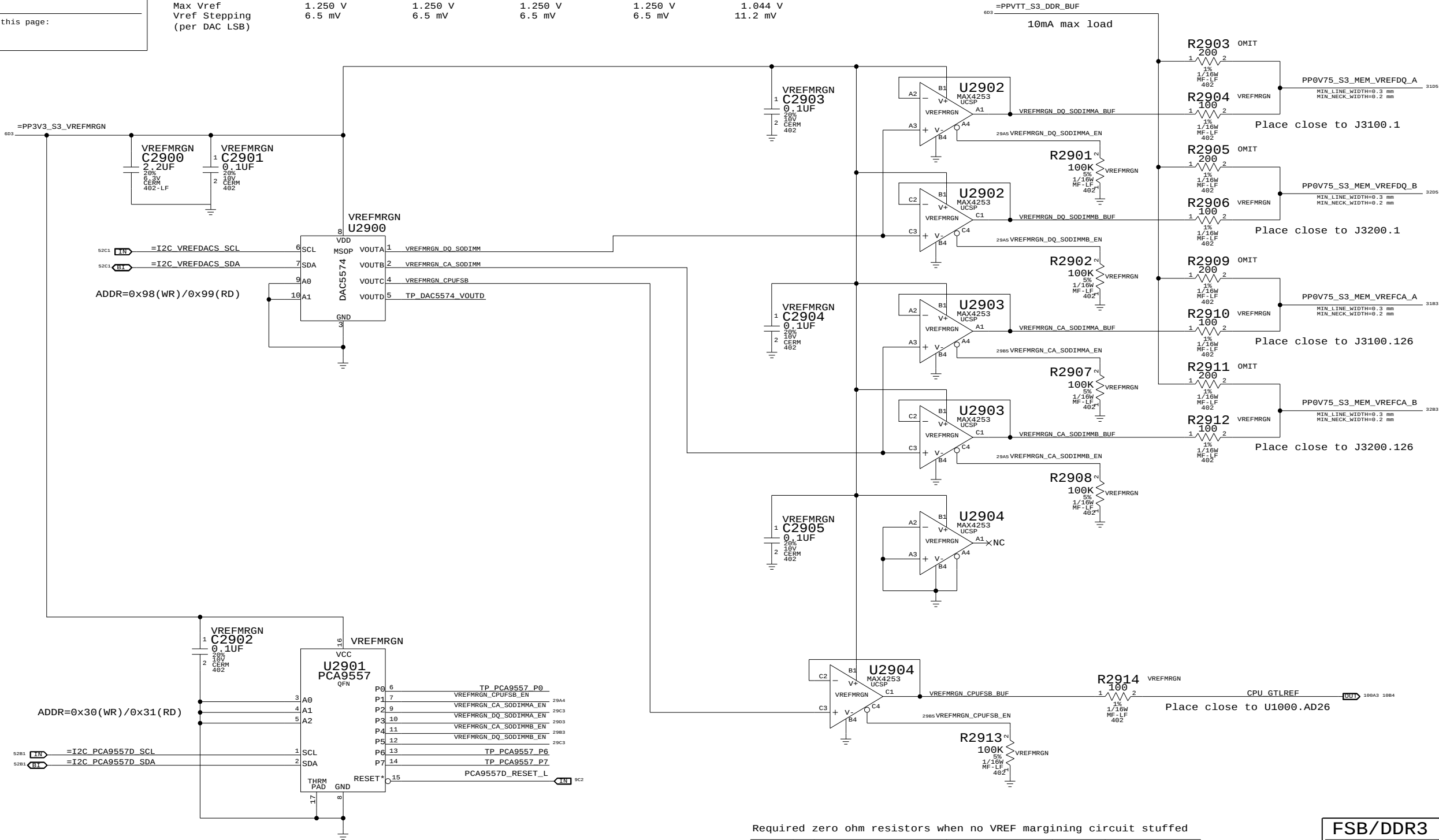
MEM A VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF DQ
A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

MEM B VREF CA
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

CPU FSB VREF
C
0x00
0x55
-0.91 mA
0.52 mA
0.70 V
0.091 V
1.044 V
11.2 mV

S0-DIMM A and S0-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0149	1	RES, 402, 1/16W, 200 OHM, 1%	R2903		VREFMRGN
116S0004	1	RES, 402, 1/16W, 0 OHM, 5%	R2903		PRODUCTION
114S0149	1	RES, 402, 1/16W, 200 OHM, 1%	R2905		VREFMRGN
116S0004	1	RES, 402, 1/16W, 0 OHM, 5%	R2905		PRODUCTION
114S0149	1	RES, 402, 1/16W, 200 OHM, 1%	R2909		VREFMRGN
116S0004	1	RES, 402, 1/16W, 0 OHM, 5%	R2909		PRODUCTION
114S0149	1	RES, 402, 1/16W, 200 OHM, 1%	R2911		VREFMRGN
116S0004	1	RES, 402, 1/16W, 0 OHM, 5%	R2911		PRODUCTION

FSB/DDR3 Vref Margining

SYNC_MASTER=AARON SYNC_DATE=05/05/2008

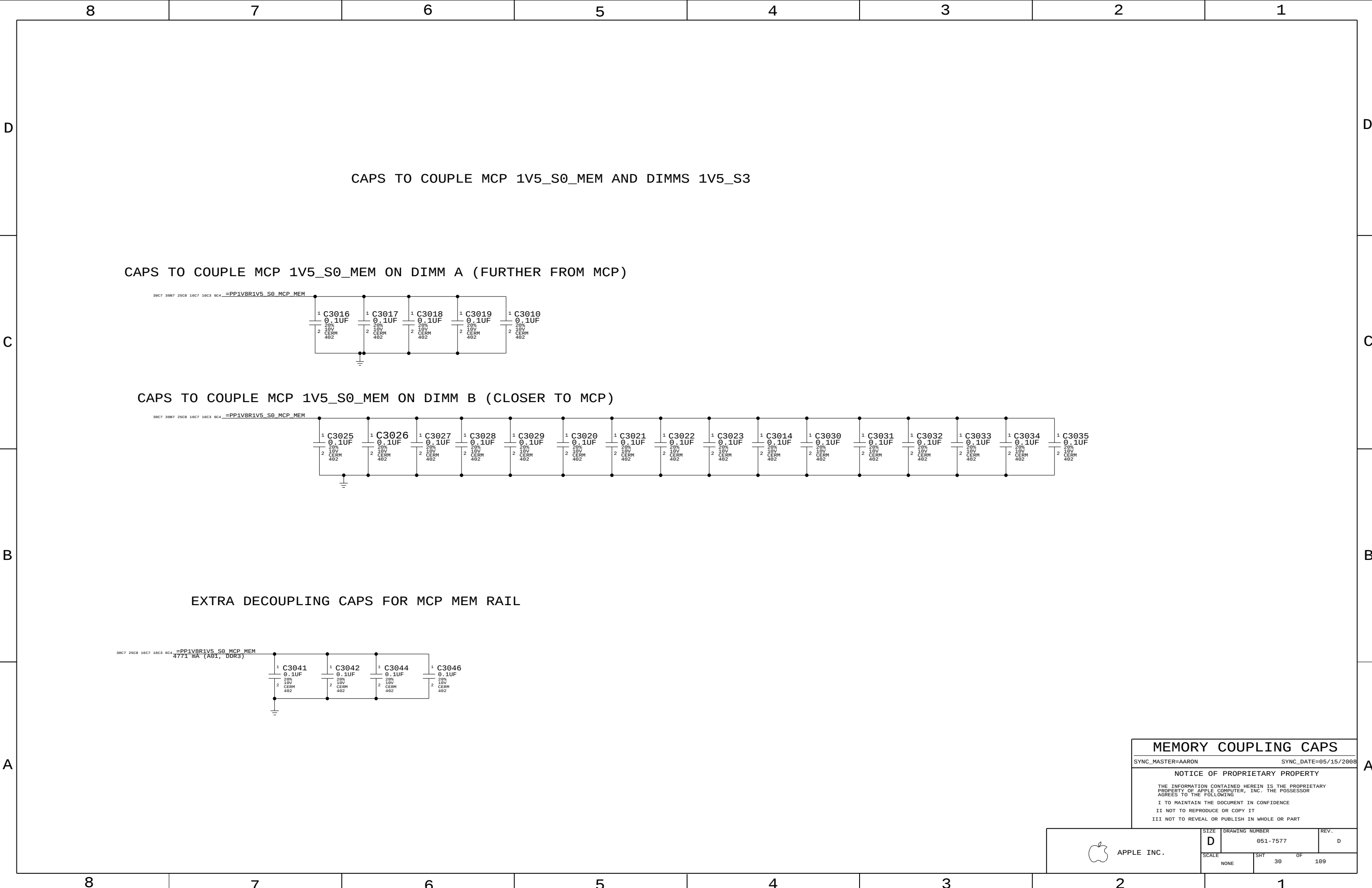
NOTICE OF PROPRIETARY PROPERTY

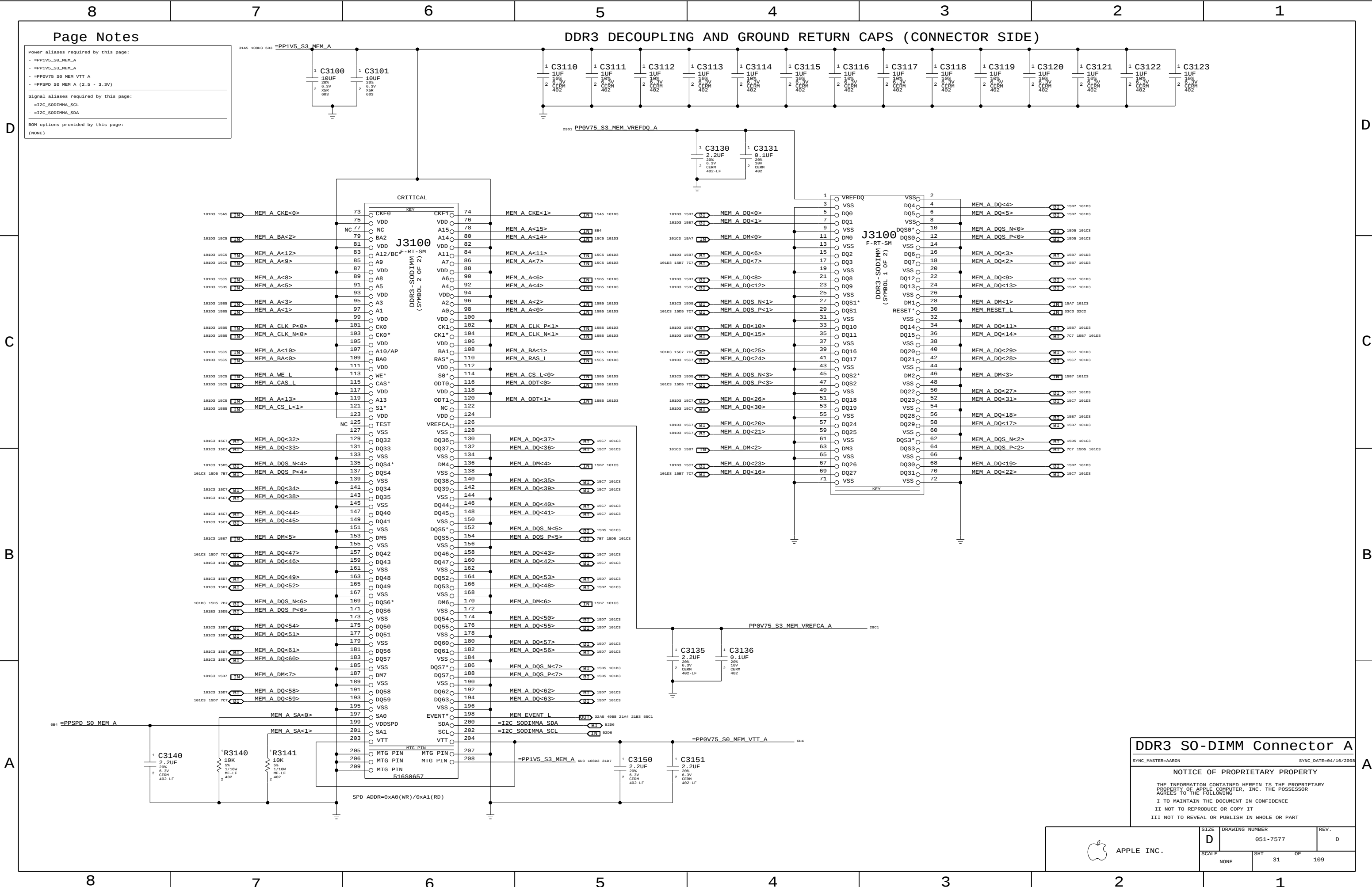
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SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	29	109





DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 SO-DIMM Connector A

SYNC_MASTER=AARON SYNC_DATE=04/16/2008

NOTICE OF PROPRIETARY PROPERTY

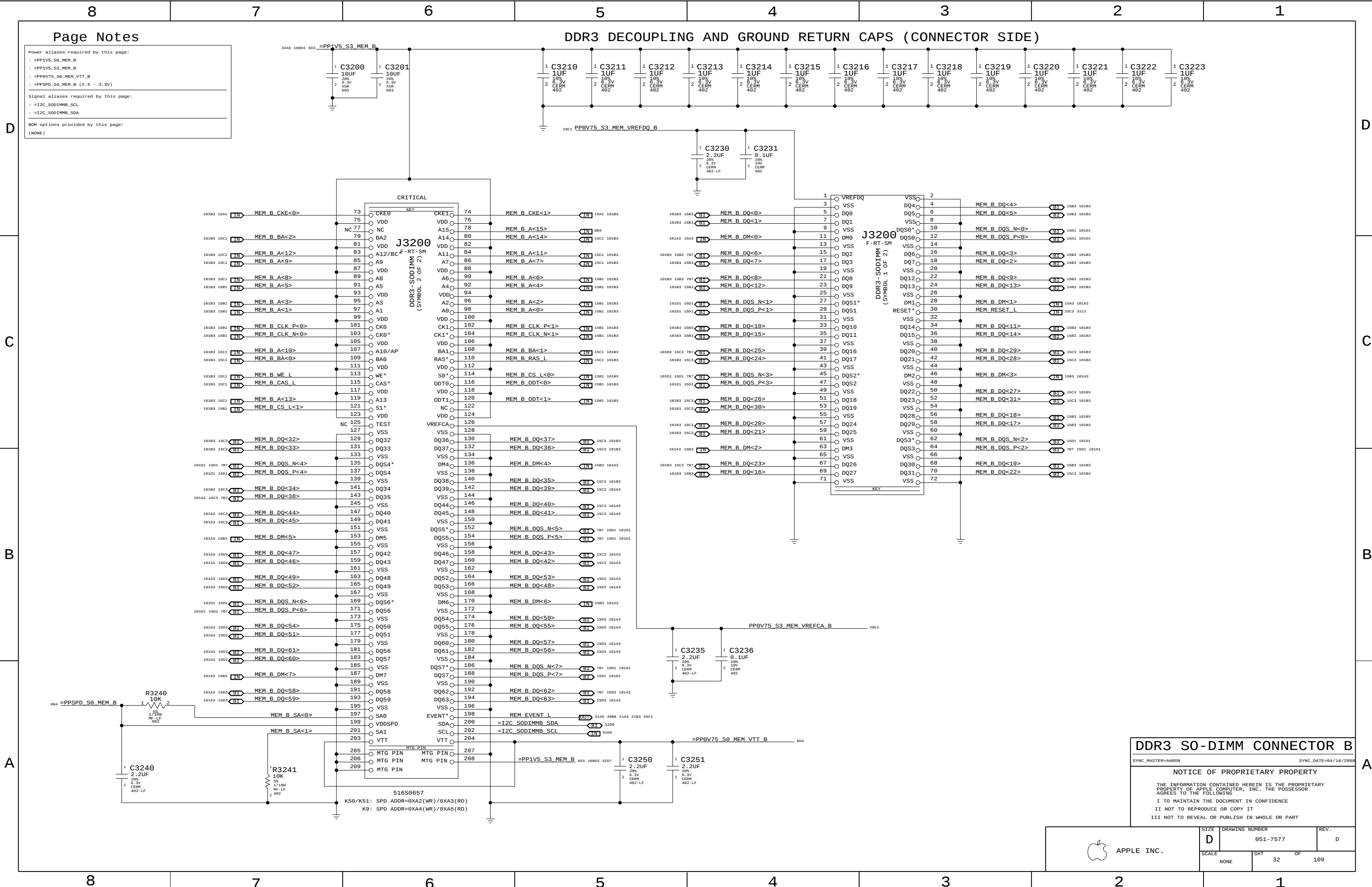
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7577	D
SCALE		SHT	OF
NONE		31	109



DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:

- =PP1V5_S3_MEM_B
- =PP1V5_S0_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

DDR3 SO-DIMM CONNECTOR B

SYNC_MASTER=AARON SYNC_DATE=04/16/2008

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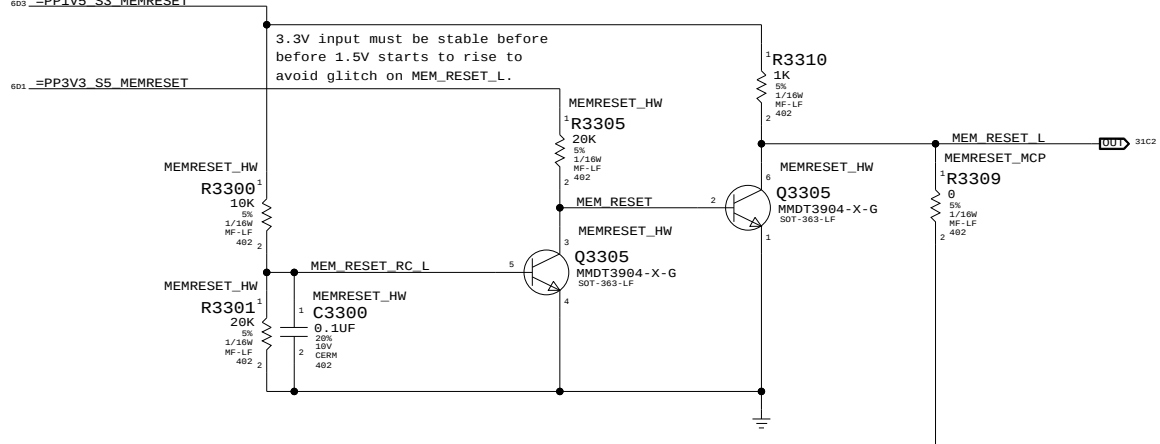
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7577	D
SCALE		SHT	OF
NONE		32	109

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support
SYNC_MASTER=T18_AARON SYNC_DATE=09/03/2008

SYNC_DATE=09/03/2008

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	SIZE	DRAWING NUMBER	REV.
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D	051-7577	D
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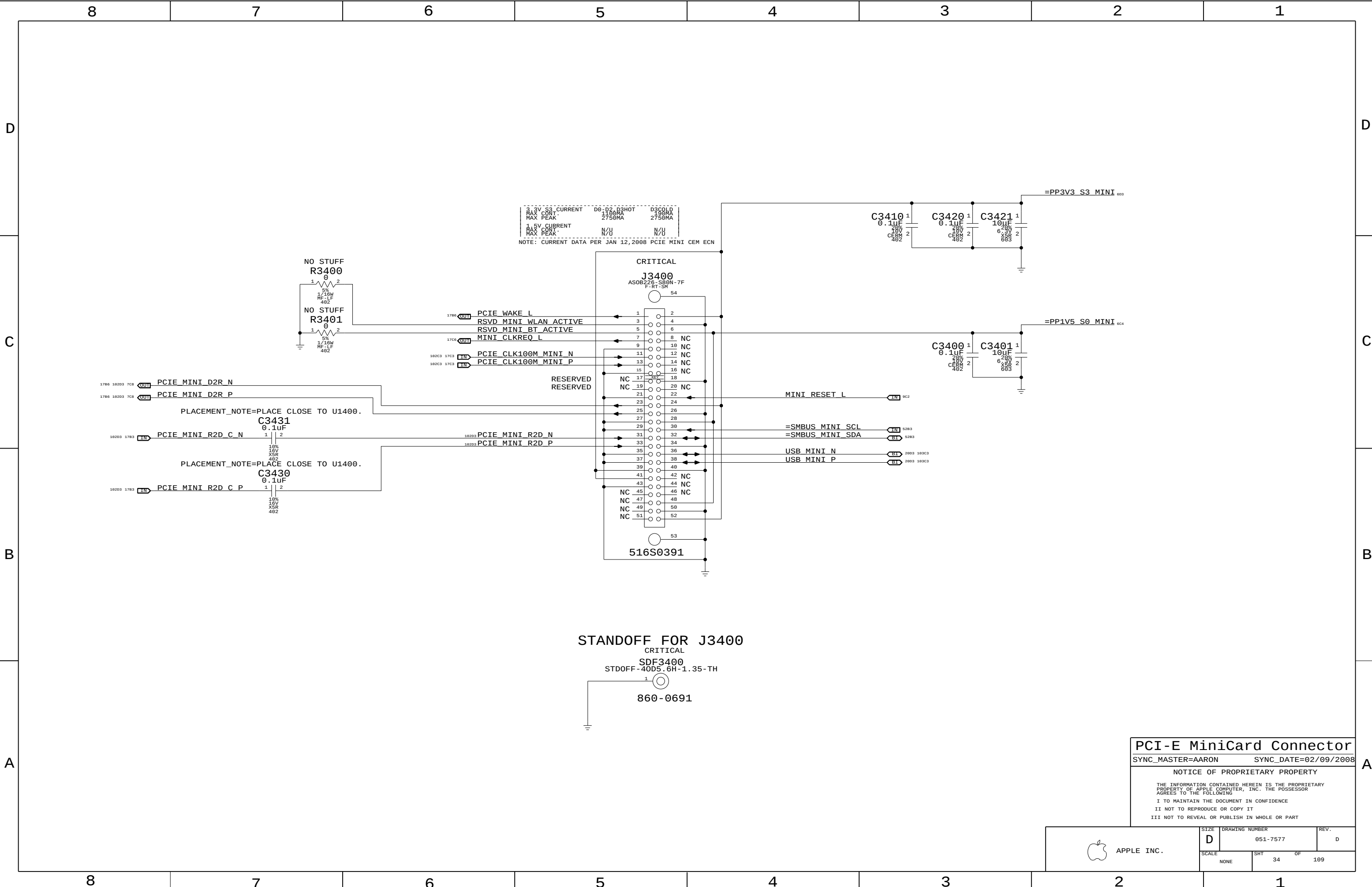
D	051-7577	D
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1.5. INC	D	381 7577	5
----------	---	----------	---

SCALE	SHT	OF
	33	100

	NONE	33	109
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1



PCI-E MiniCard Connector

SYNC_MASTER=AARON SYNC_DATE=02/09/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	34	109

D

C

B

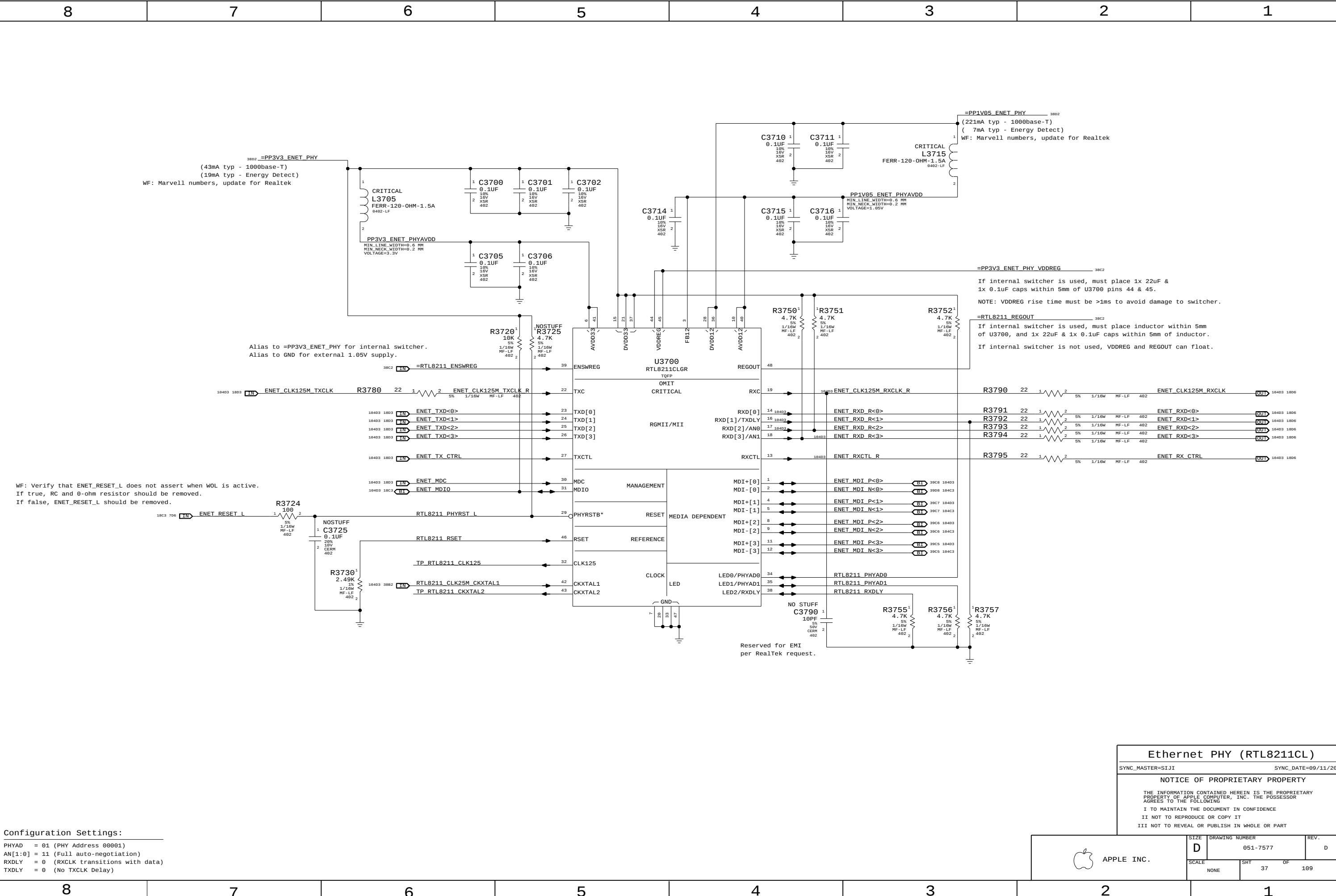
A

D

C

B

A



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

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APPLE INC.

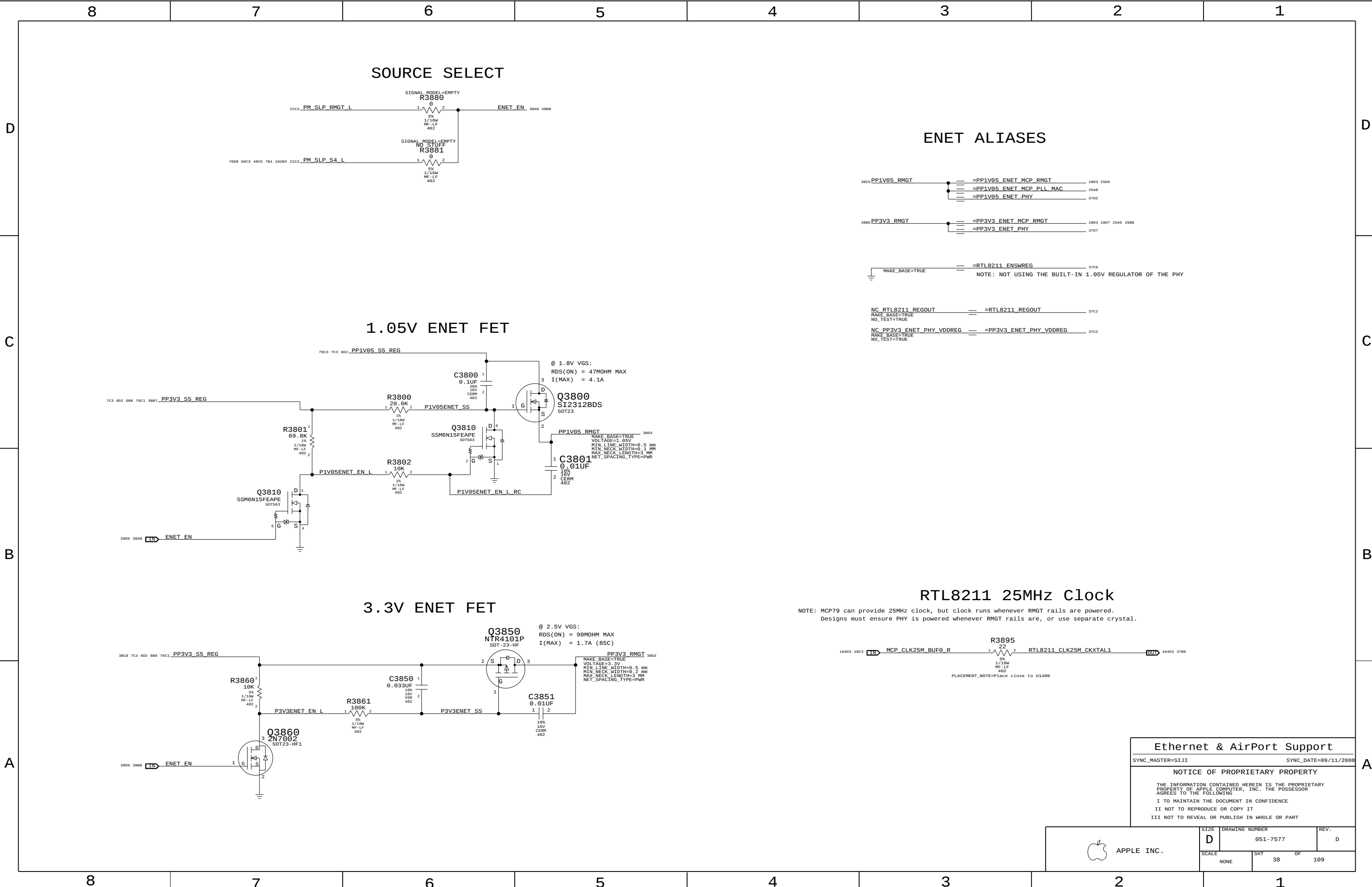
SIZE D

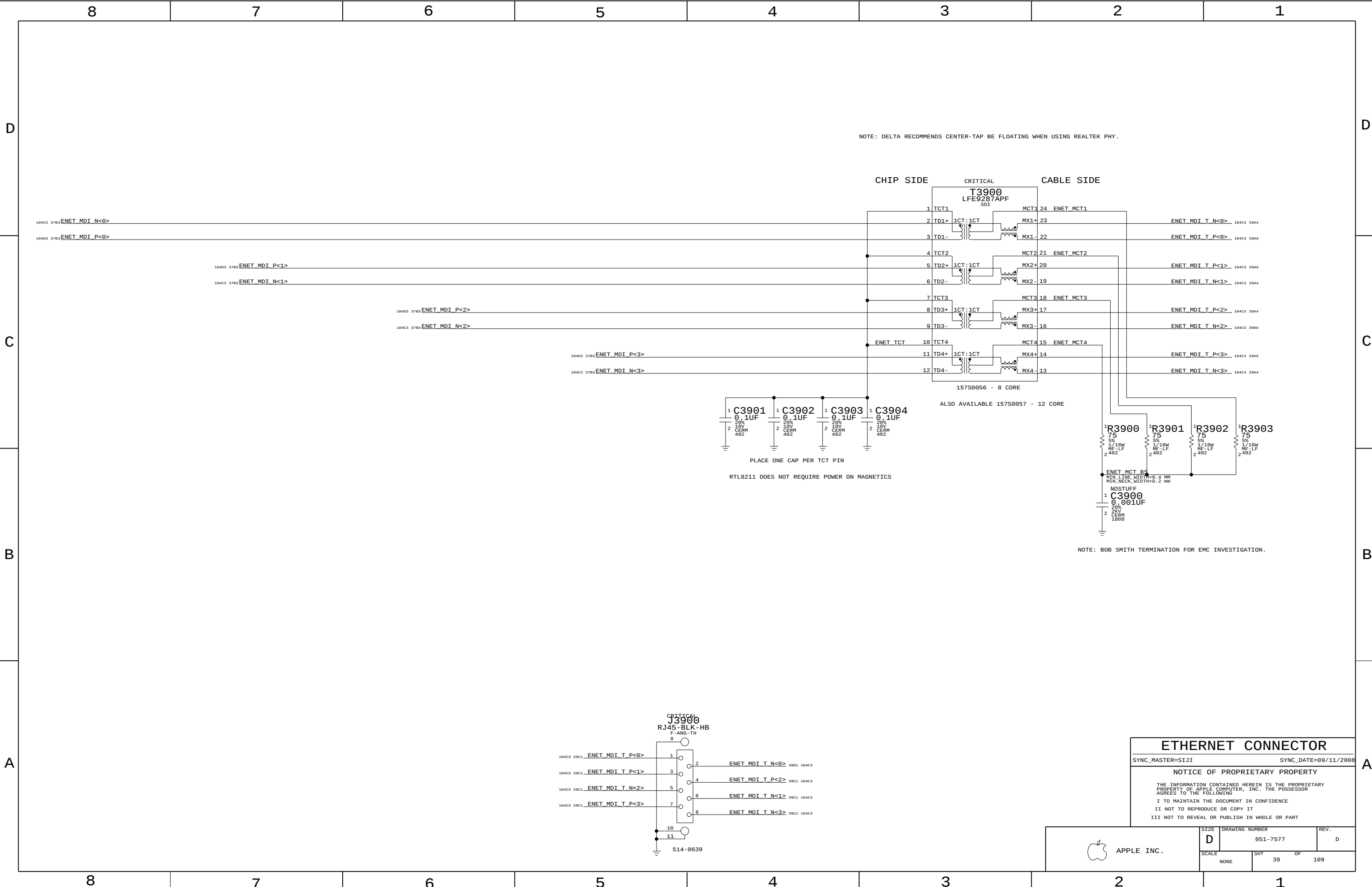
DRAWING NUMBER 051-7577

REV. D

SCALE NONE

SHT 37 OF 109





ETHERNET CONNECTOR

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

NOTICE OF PROPRIETARY PROPERTY

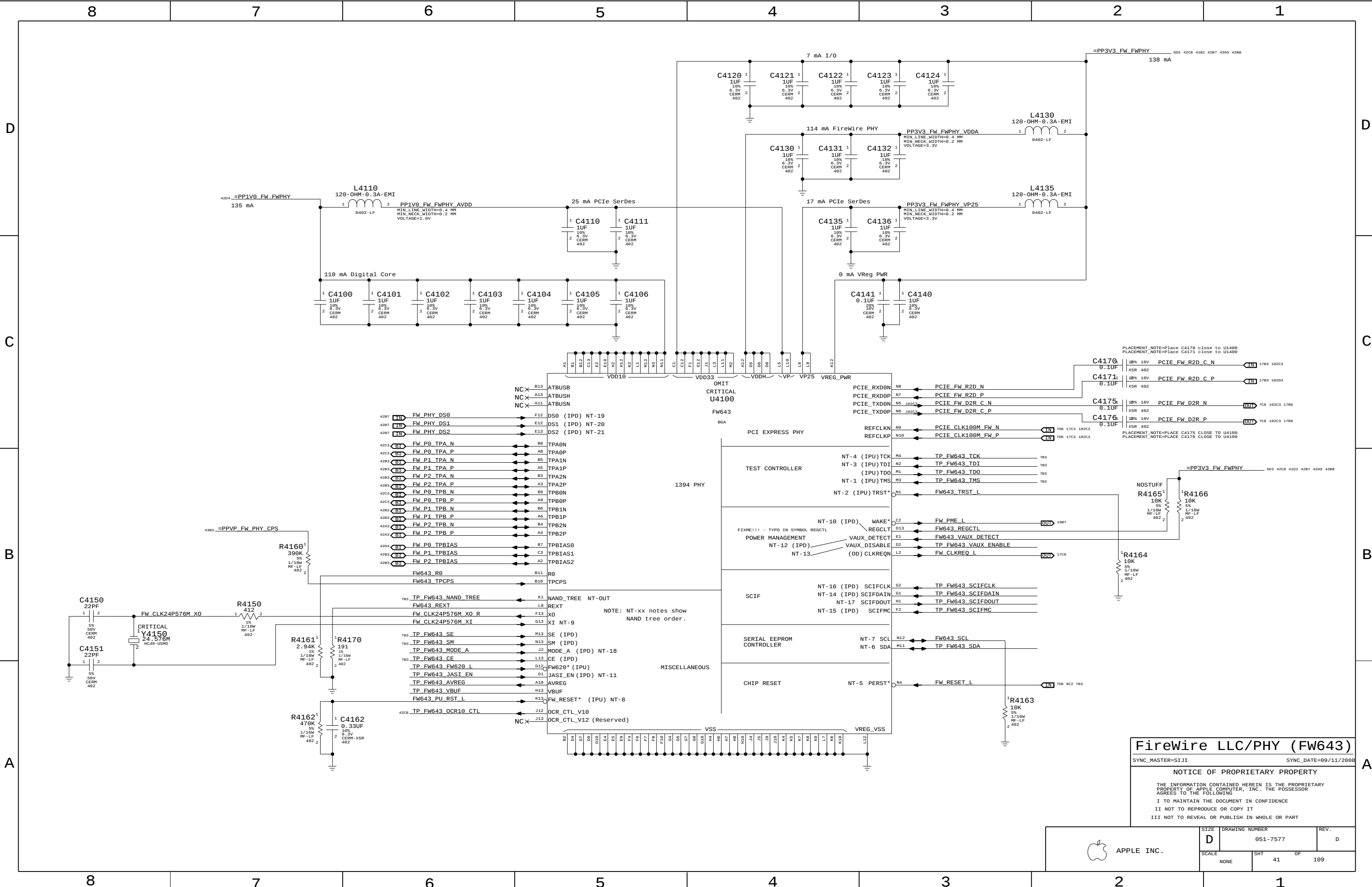
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7577	REV. D
	SCALE NONE	SHT 39	OF 109



FireWire LLC/PHY (FW643)

SYNC_MASTER=SIJII SYNC_DATE=09/11/2008

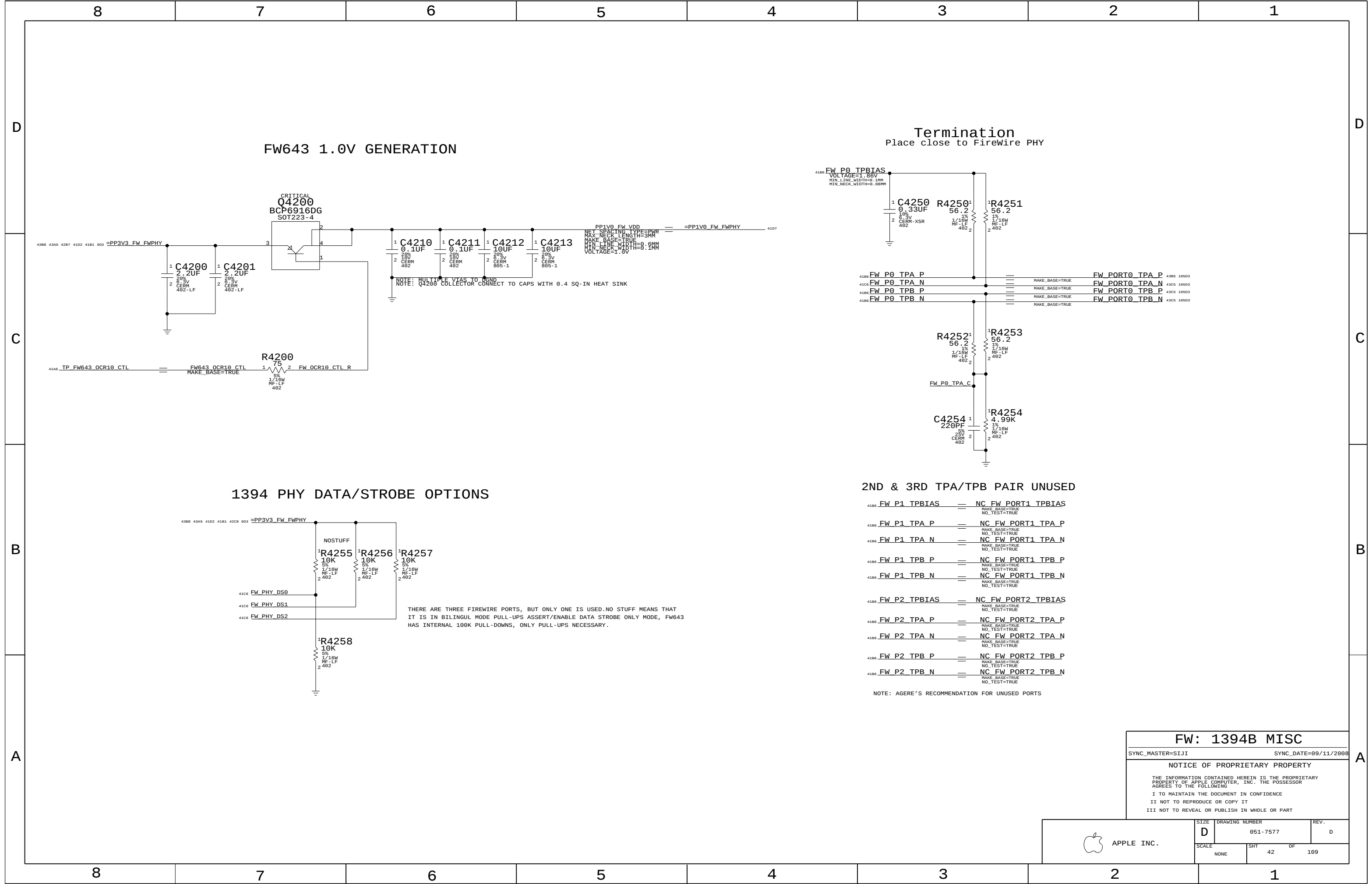
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	41	109



FW643 1.0V GENERATION

Termination
Place close to FireWire PHY

1394 PHY DATA/STROBE OPTIONS

2ND & 3RD TPA/TPB PAIR UNUSED

FW: 1394B MISC

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

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APPLE INC.

SIZE D

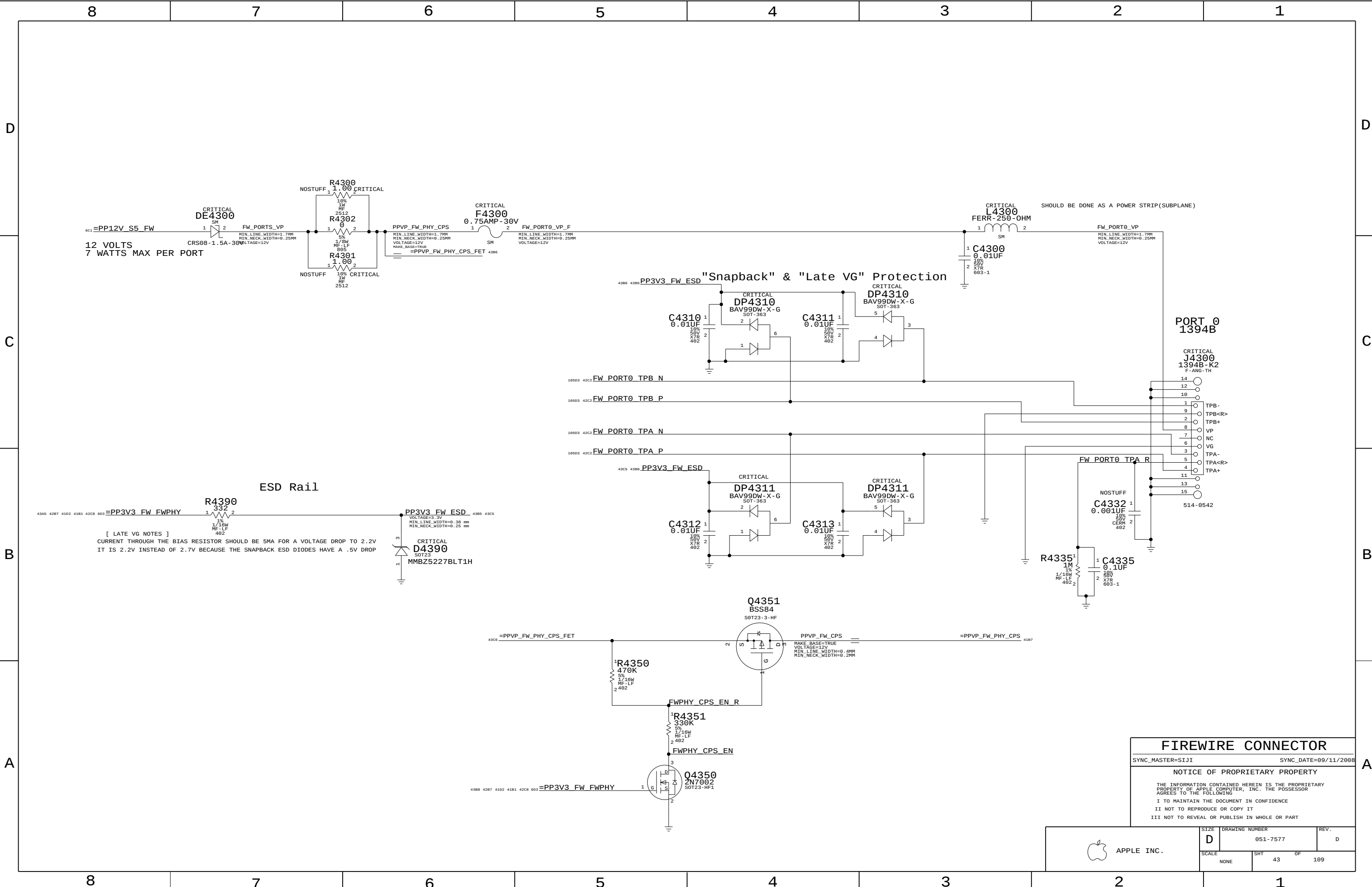
DRAWING NUMBER 051-7577

REV. D

SCALE NONE

SHT 42

OF 109



FIREWIRE CONNECTOR

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

NOTICE OF PROPRIETARY PROPERTY

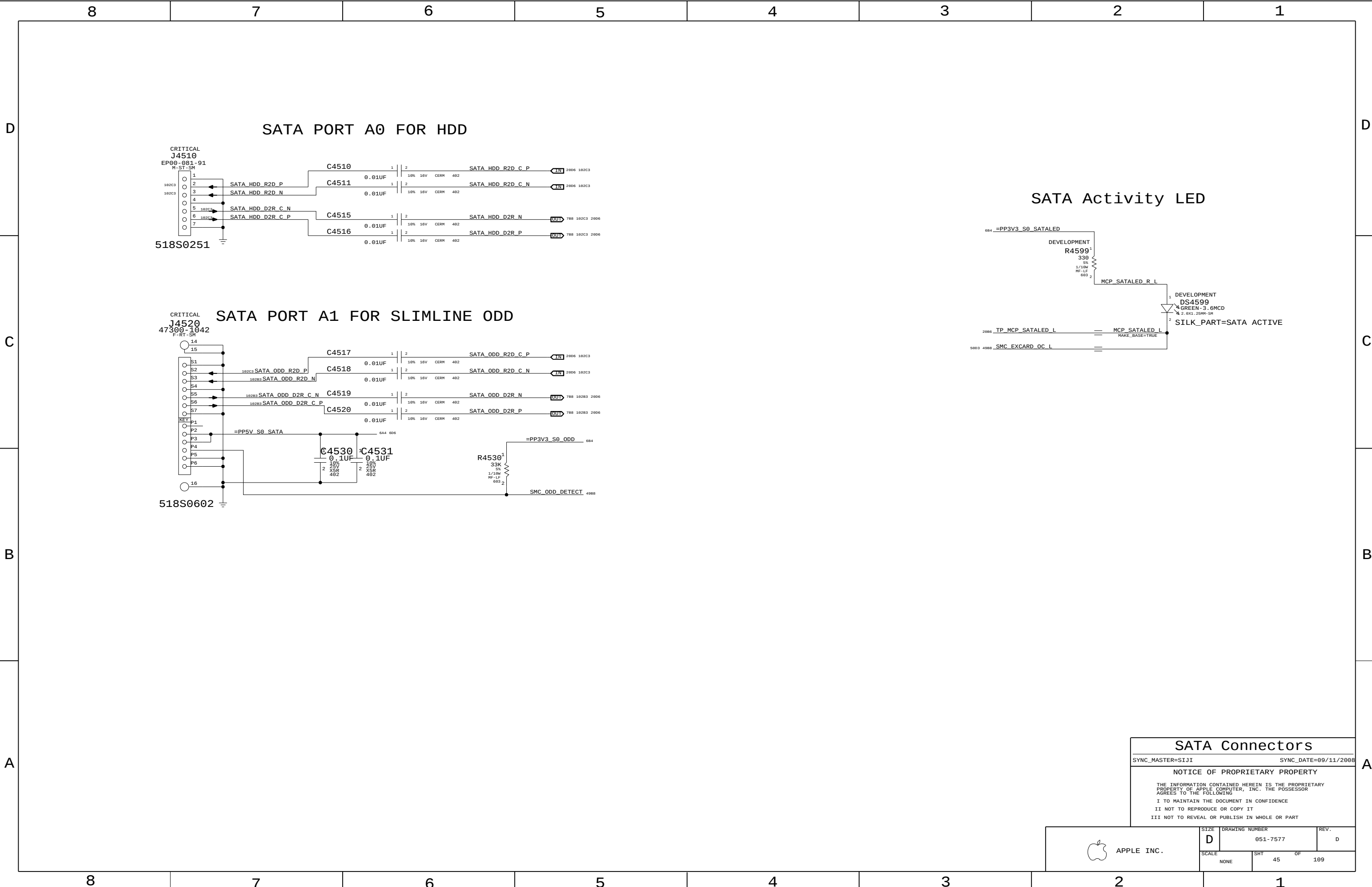
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7577	D
SCALE		SHT	OF
NONE		43	109



SATA Connectors

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

NOTICE OF PROPRIETARY PROPERTY

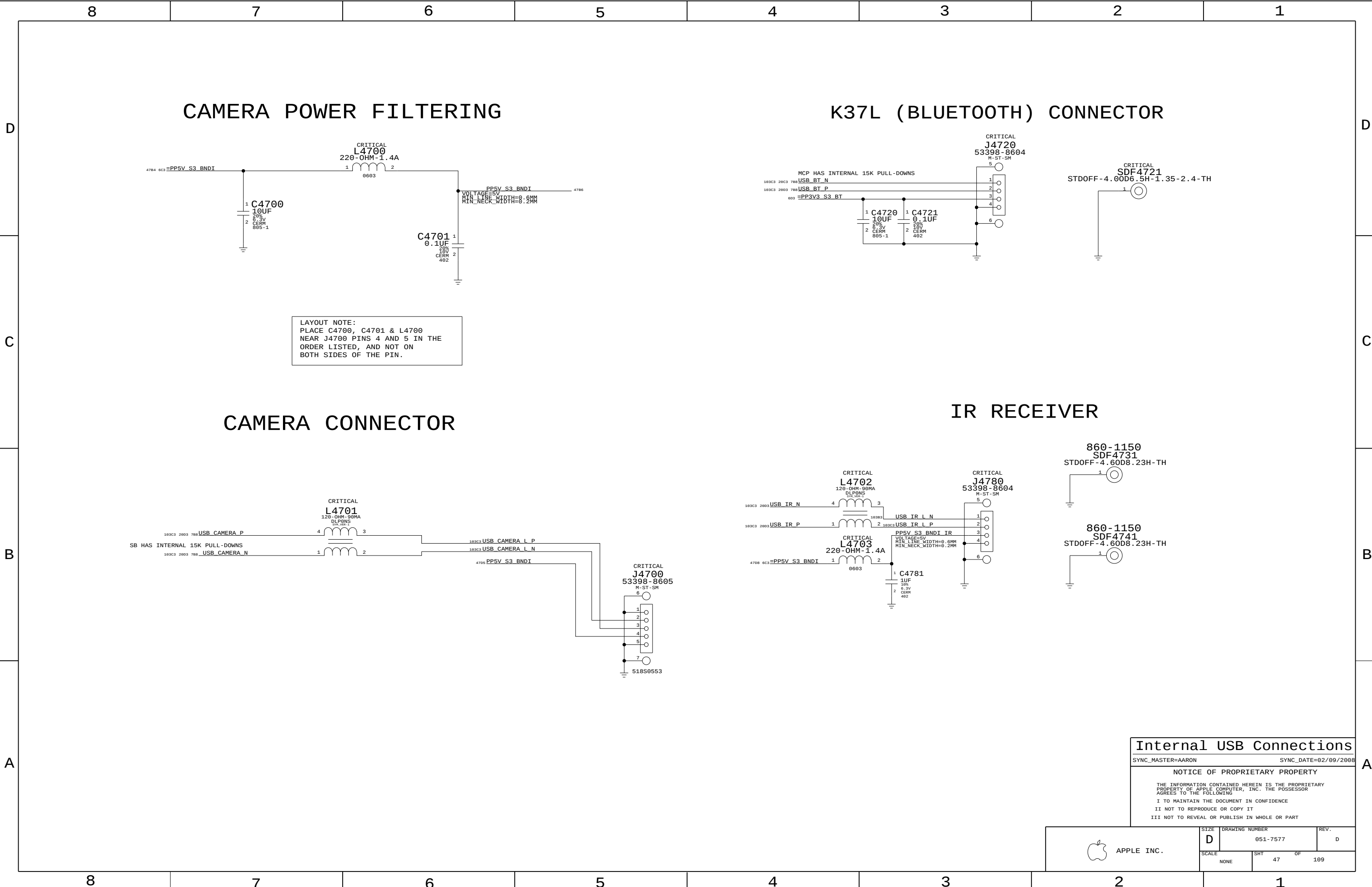
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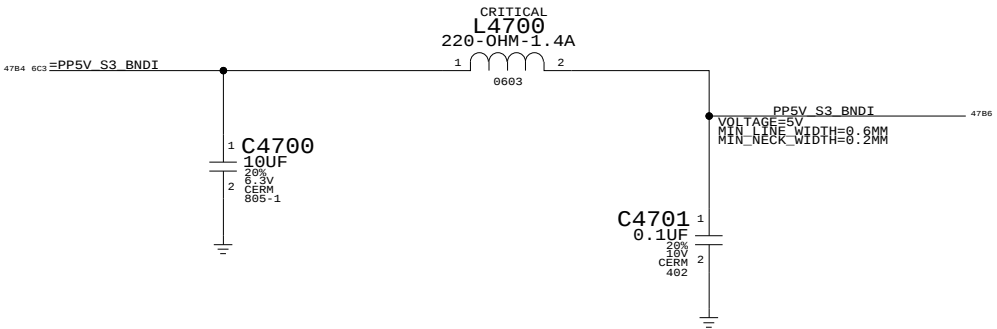
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7577	REV. D
	SCALE NONE	SHT 45	OF 109

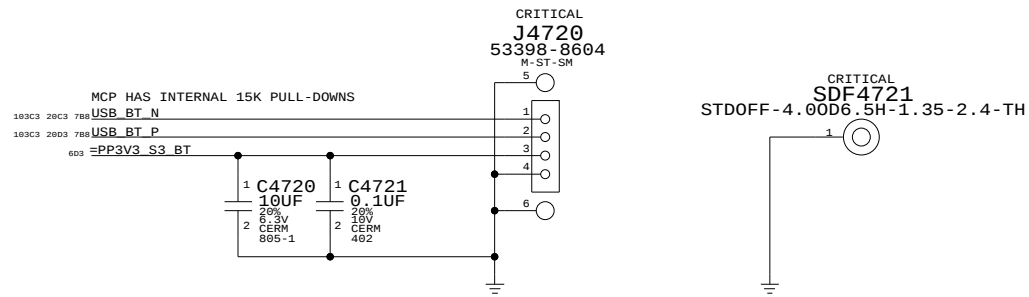


CAMERA POWER FILTERING

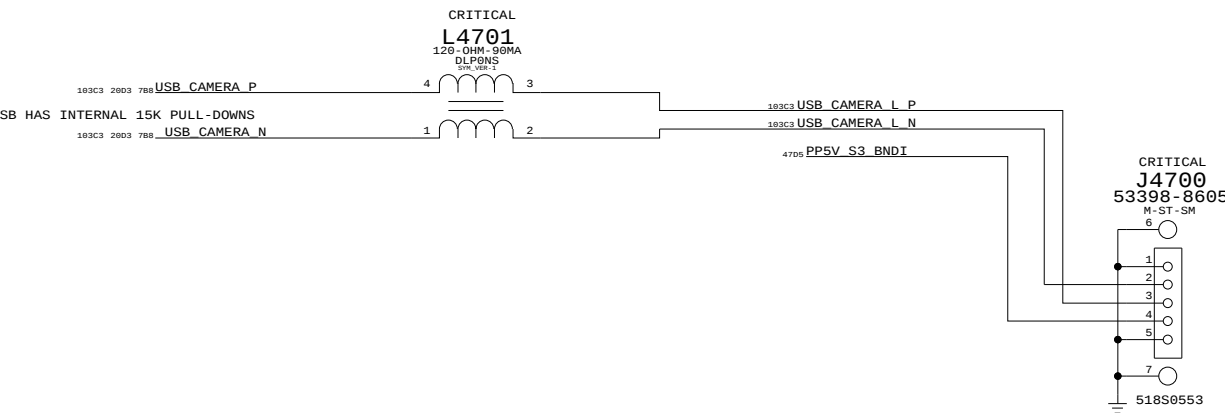


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

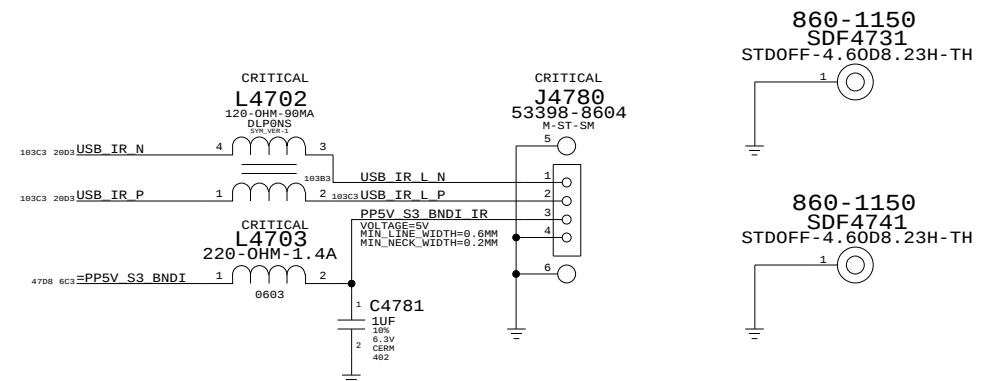
K37L (BLUETOOTH) CONNECTOR



CAMERA CONNECTOR



IR RECEIVER



Internal USB Connections

SYNC_MASTER=AARON SYNC_DATE=02/09/2008

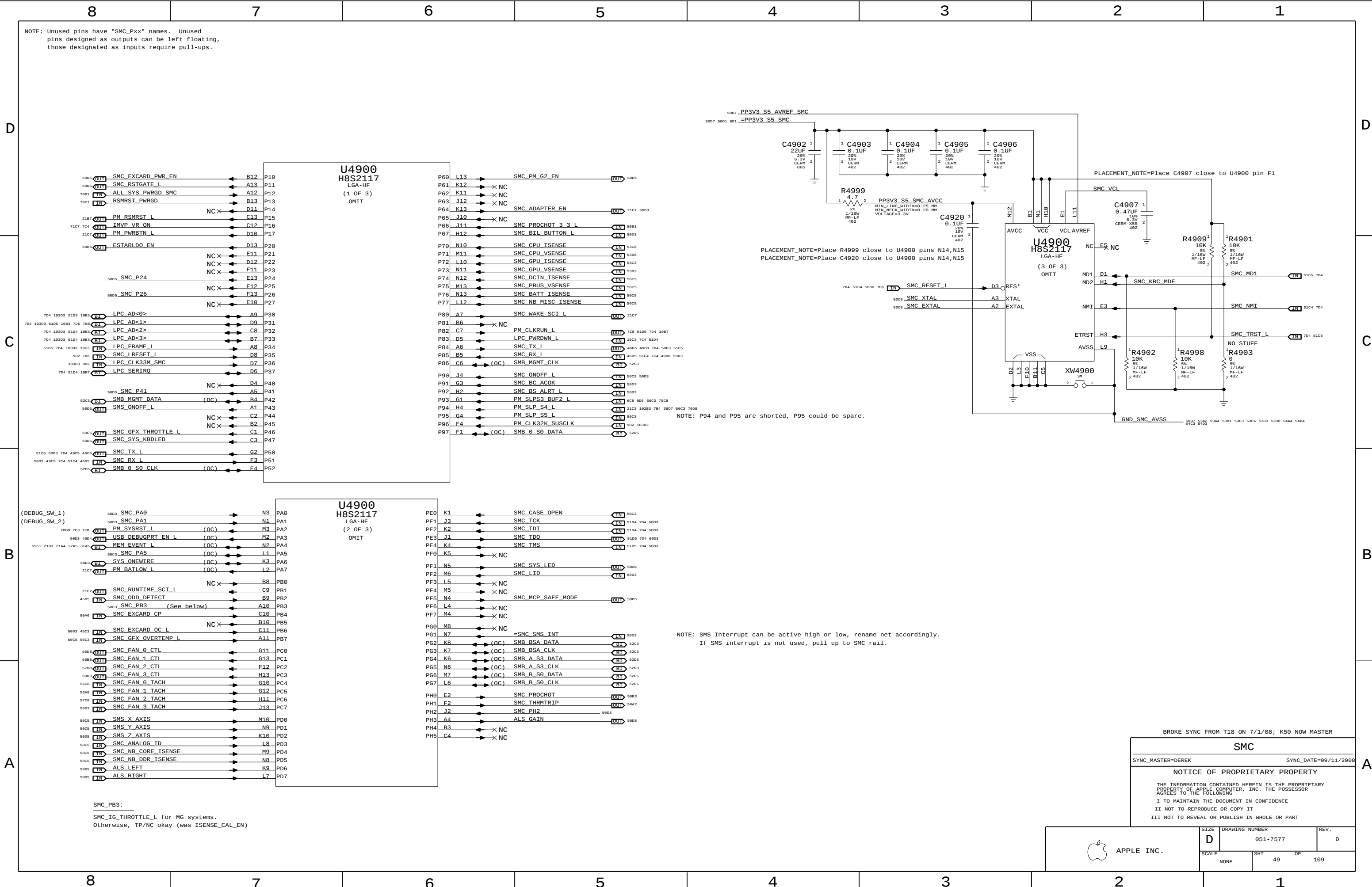
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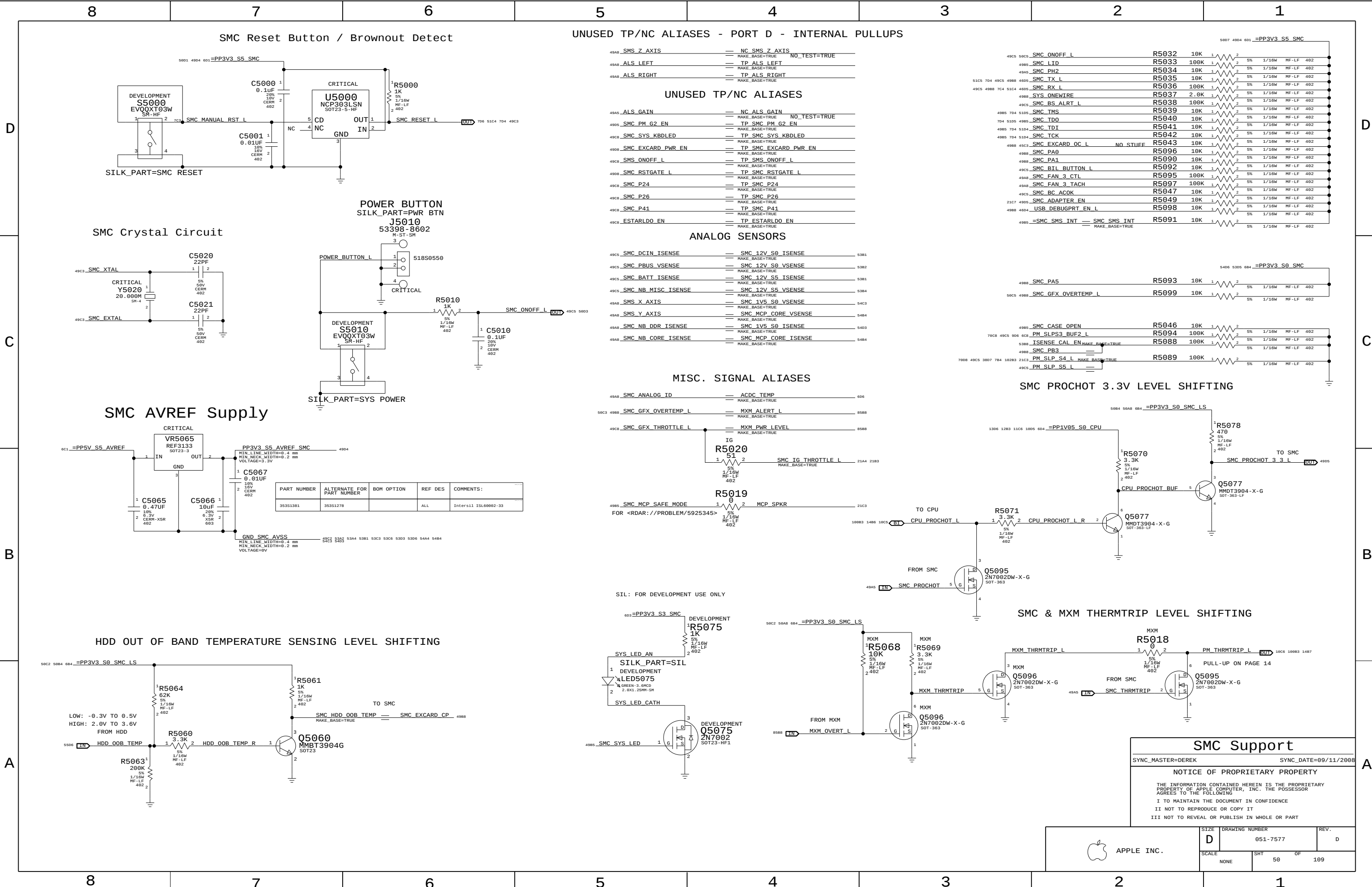
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	47	109





D

C

B

A

D

C

B

A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



C



D

C



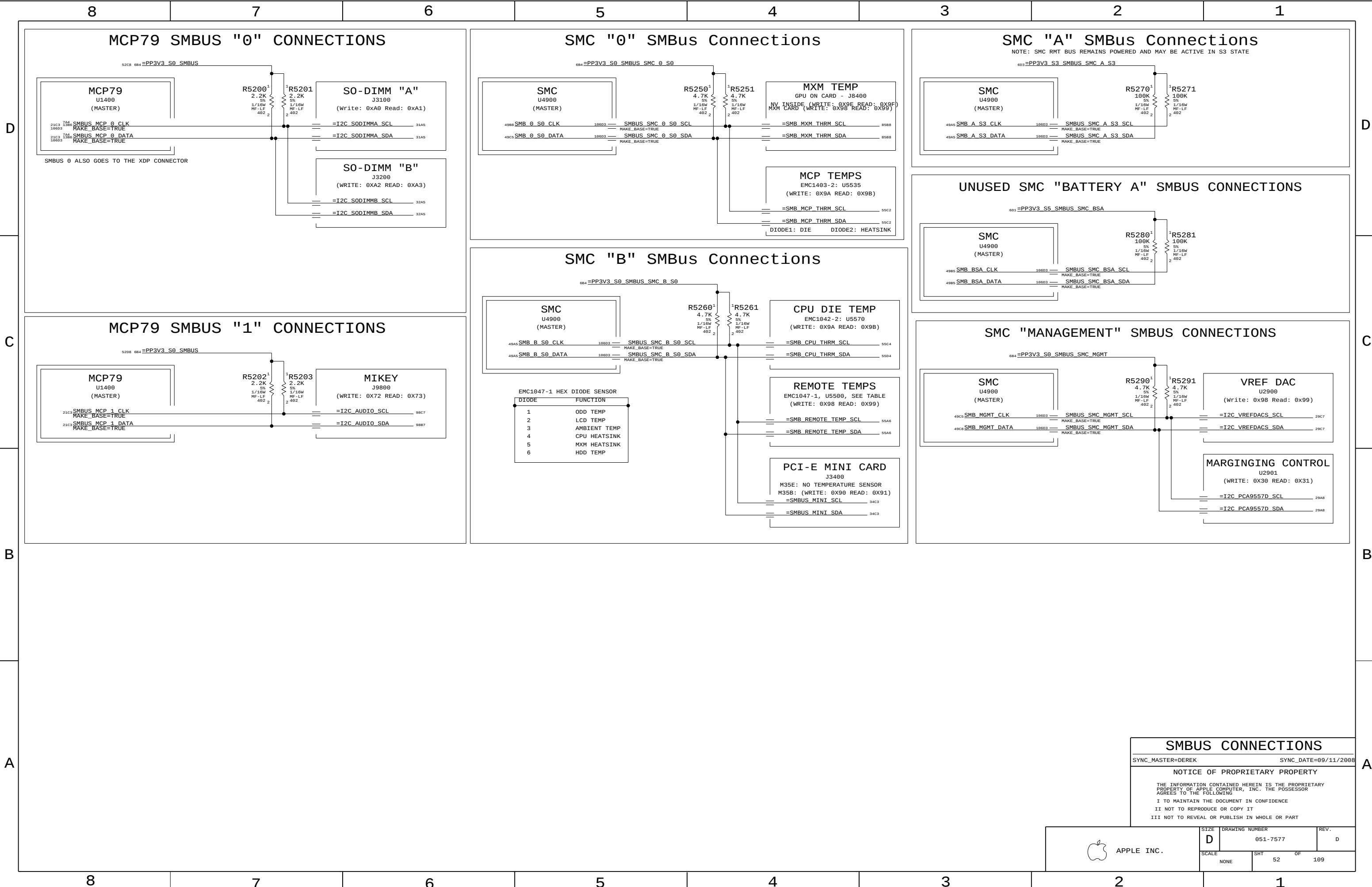
A

SYNC_MASTER=SIJI	SYNC_DATE=09/11/2008
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APPLE INC.

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



SMBUS CONNECTIONS

SYNC_MASTER=DEREK

SYNC_DATE=09/11/2008

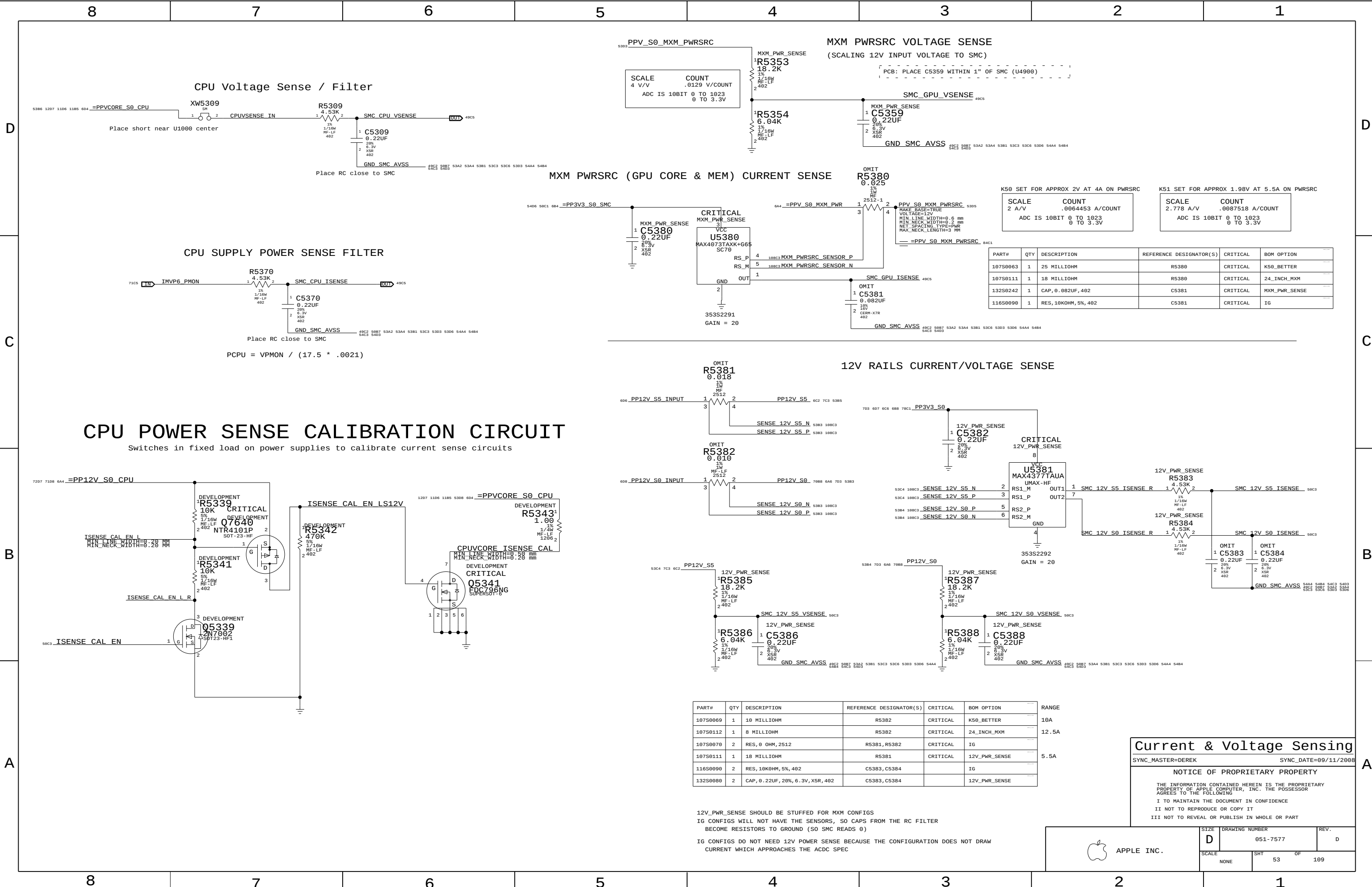
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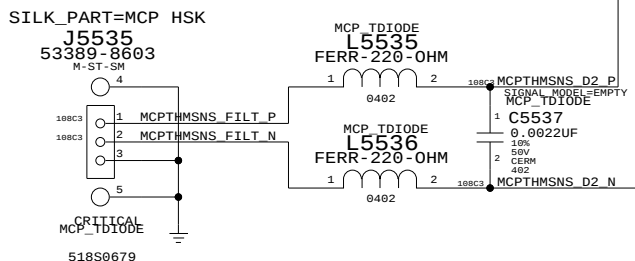
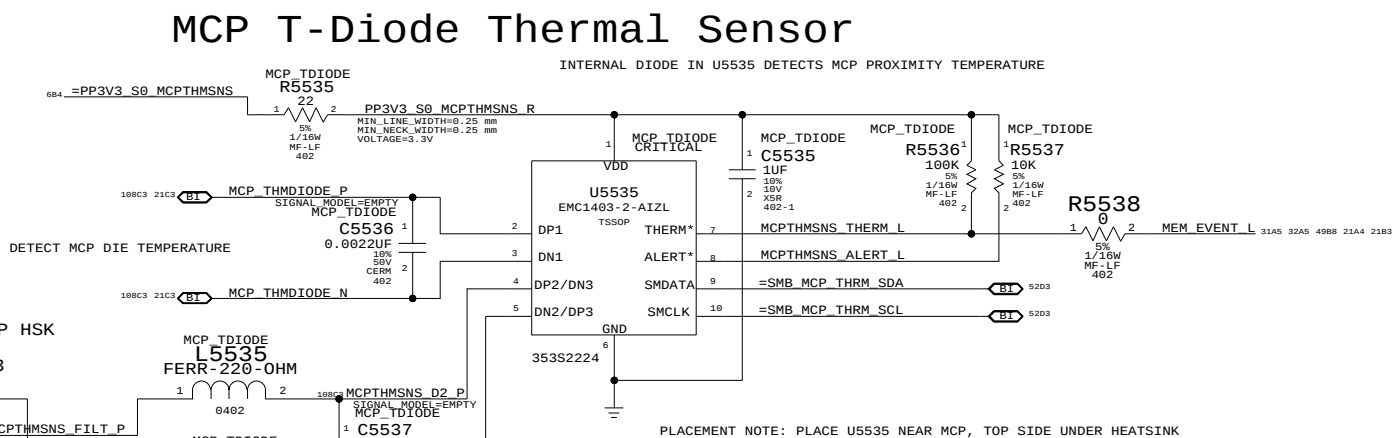
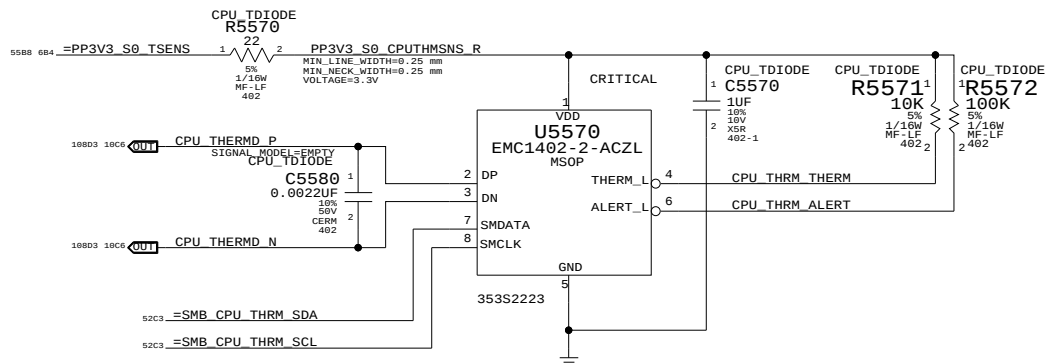
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



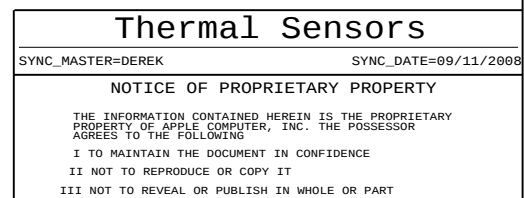
REMOTE THERMAL SENSORS

HEATSINKS, AMBIENT, PANEL AND DISKS

CPU T-Diode Thermal Sensor



REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

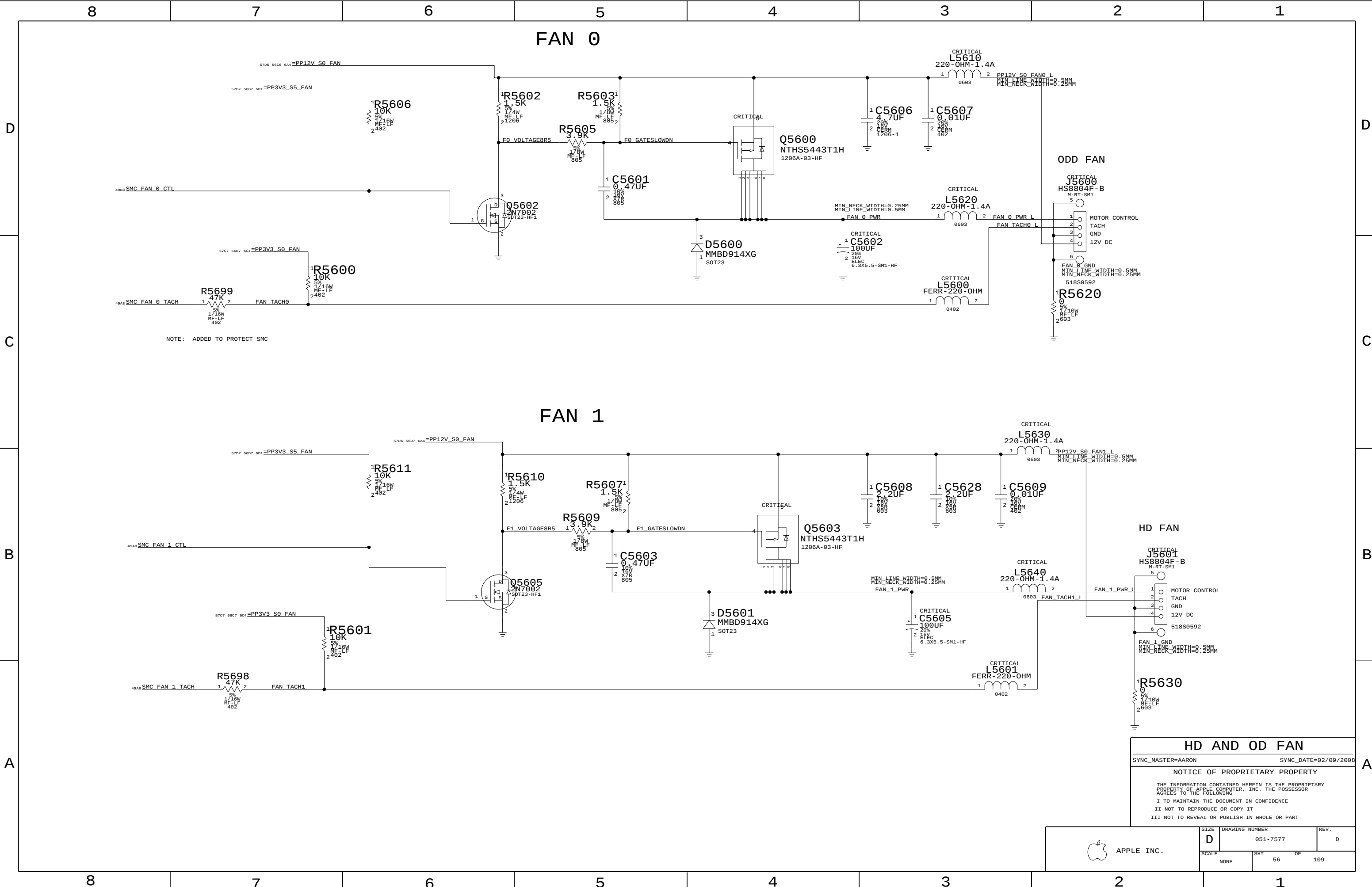


SIZE	DRAWING NUMBER	REF
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SIZE	DRAWING NUMBER	RE
D	051-7577	

SCALE	SHT	OF
	55	100

NONE	55	109
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NOTE: ADDED TO PROTECT SMC

HD AND OD FAN

SYNC_MASTER=AARON SYNC_DATE=02/09/2008

NOTICE OF PROPRIETARY PROPERTY

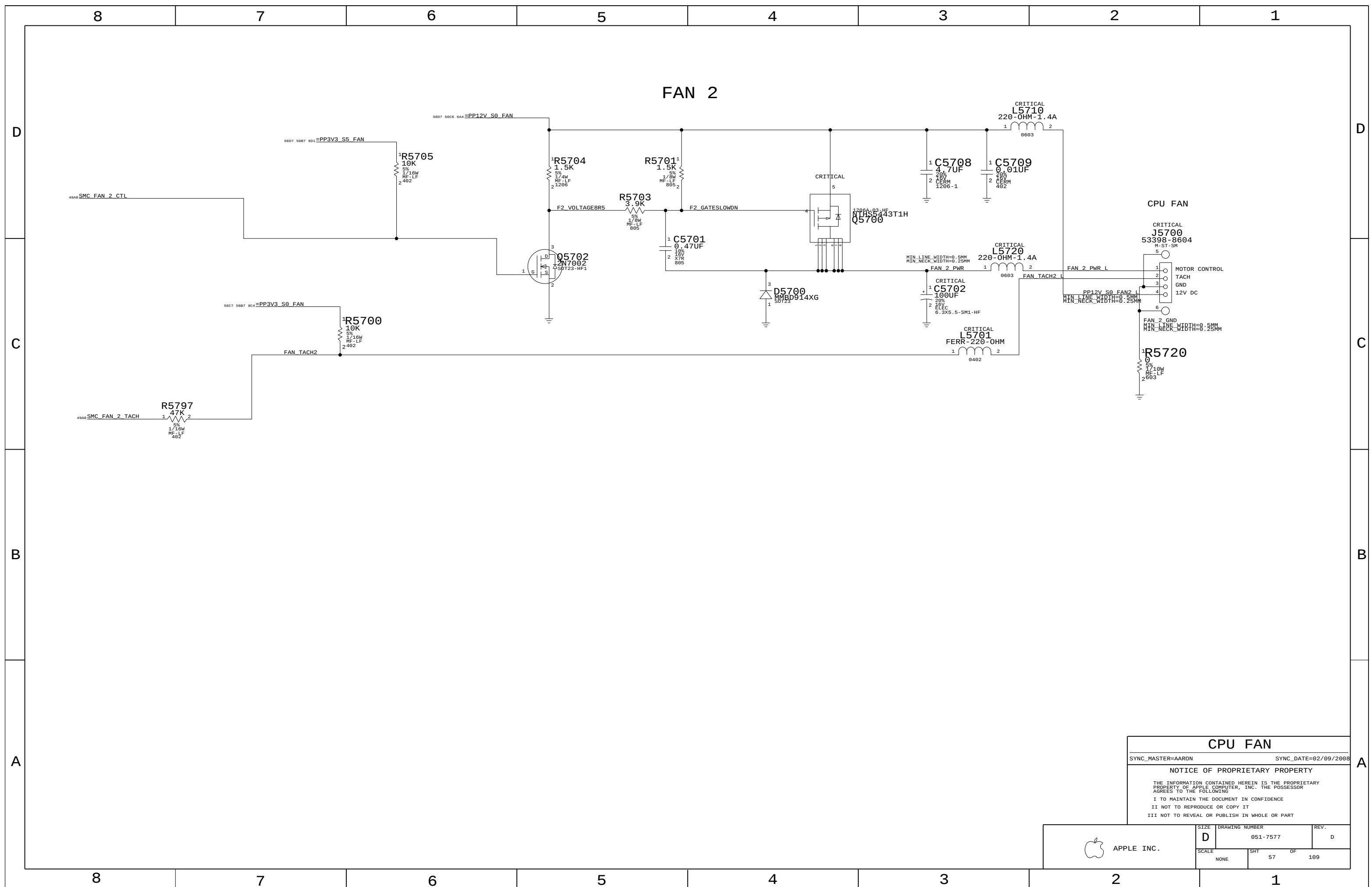
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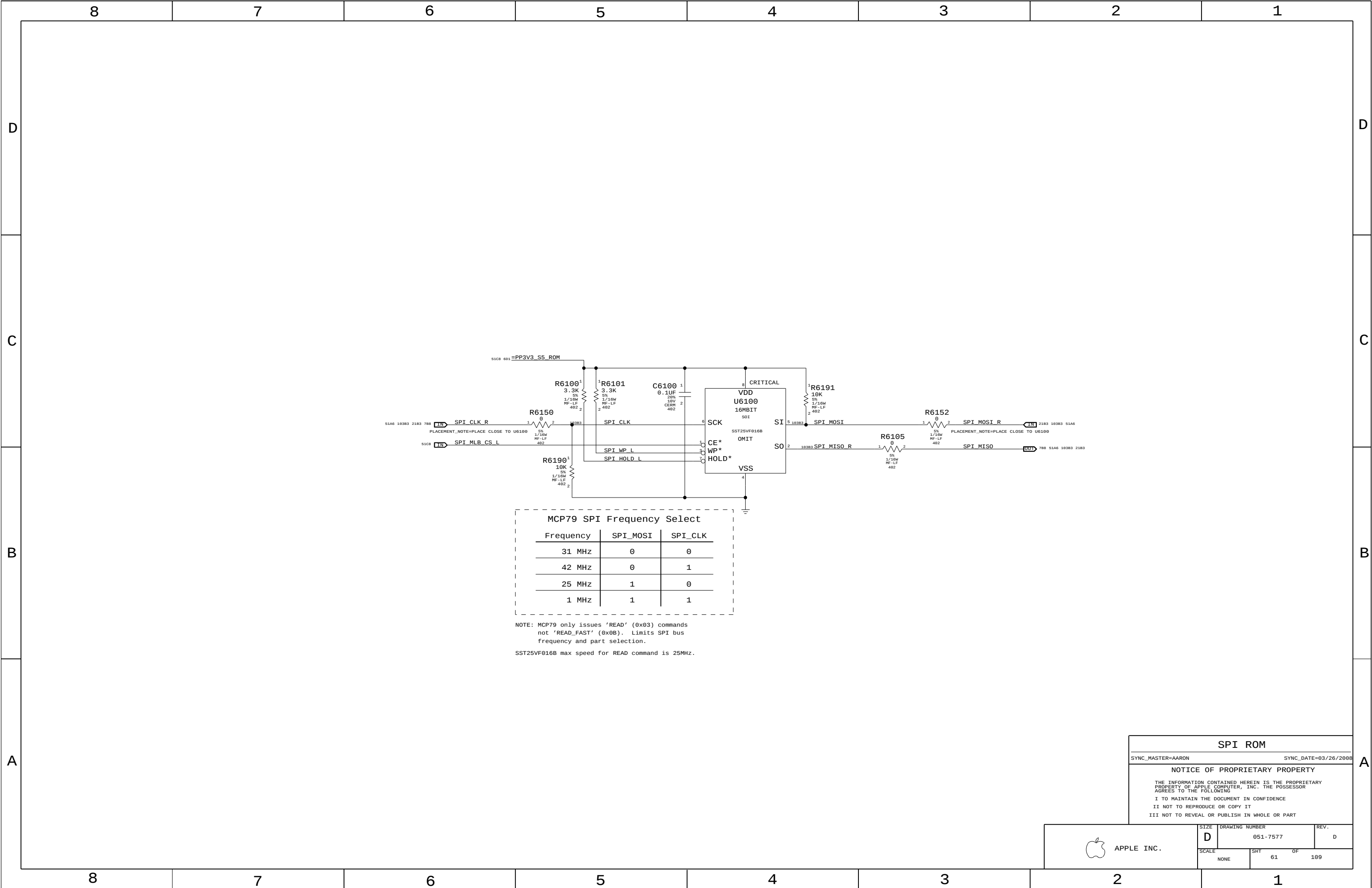
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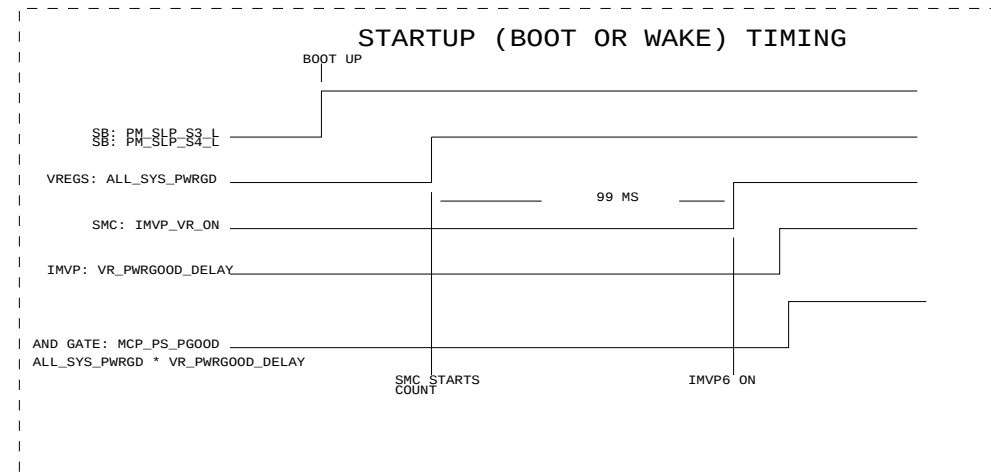
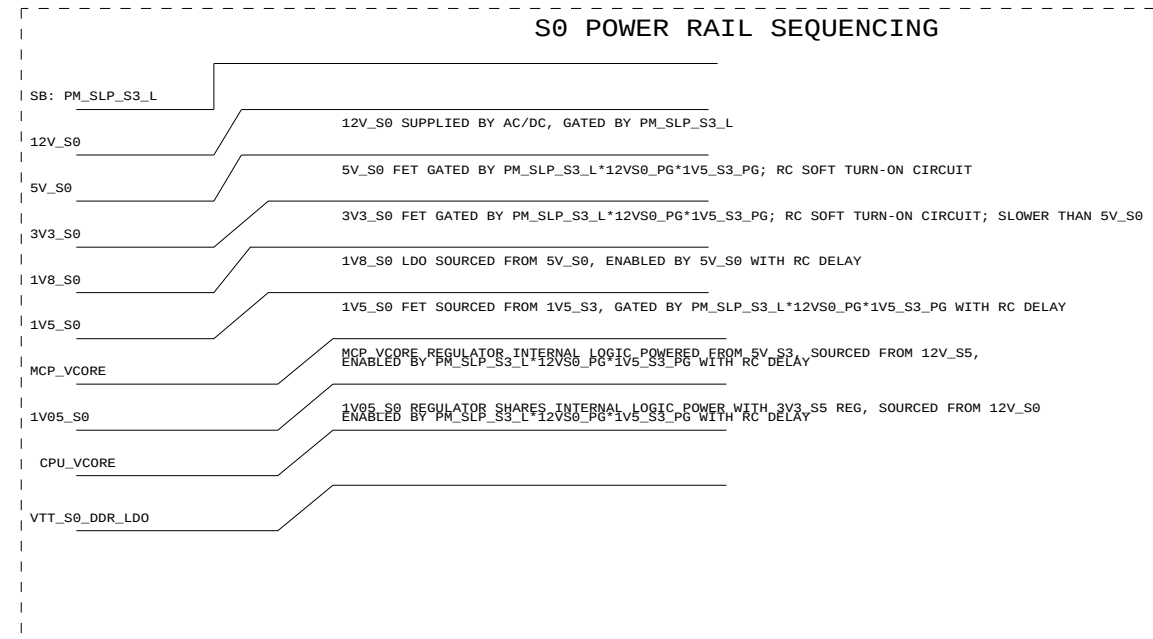
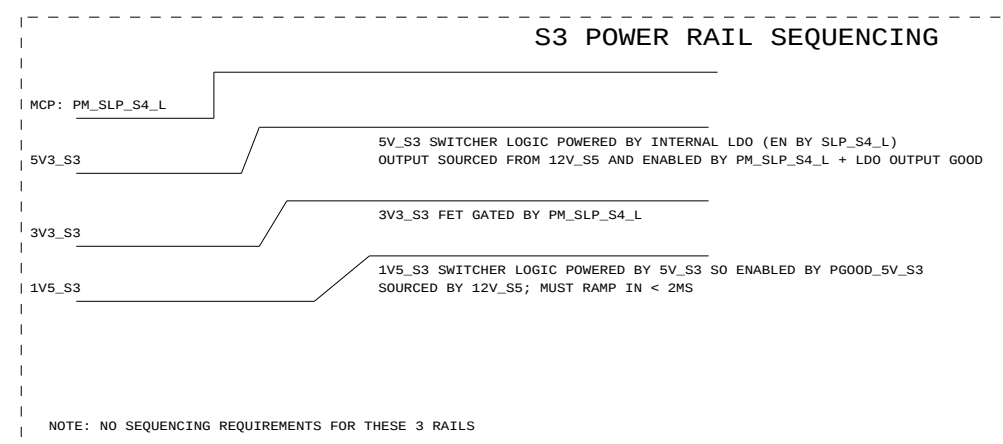
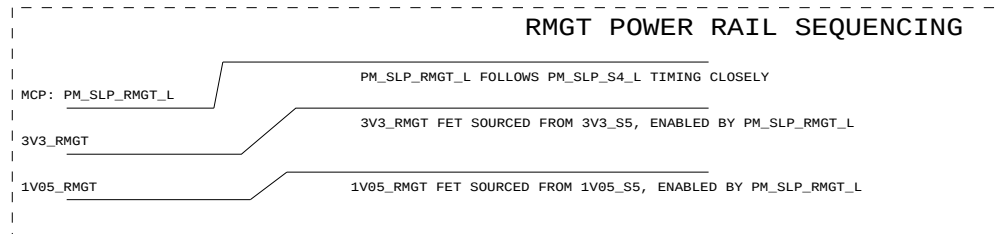
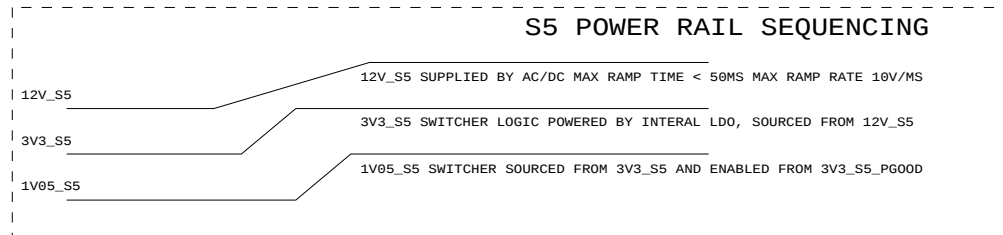
II NOT TO REPRODUCE OR COPY IT

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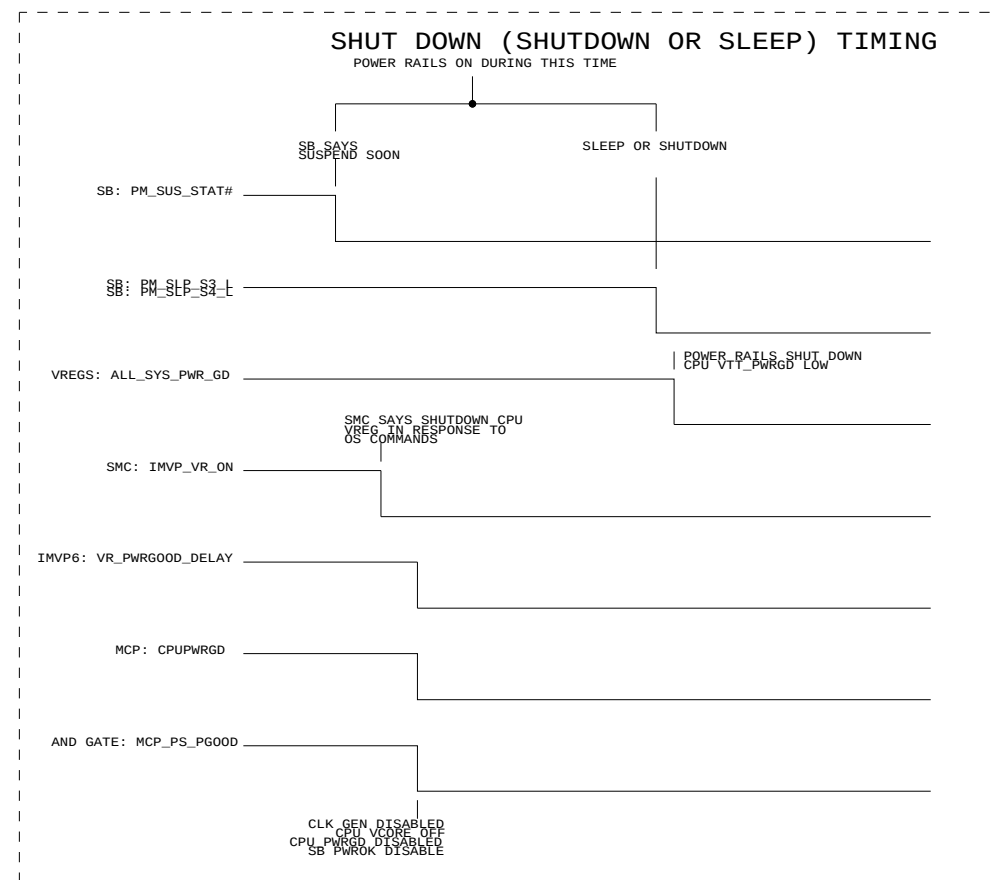
APPLE INC.	SIZE D	DRAWING NUMBER 051-7577	REV. D
	SCALE NONE	SHT 56	OF 109

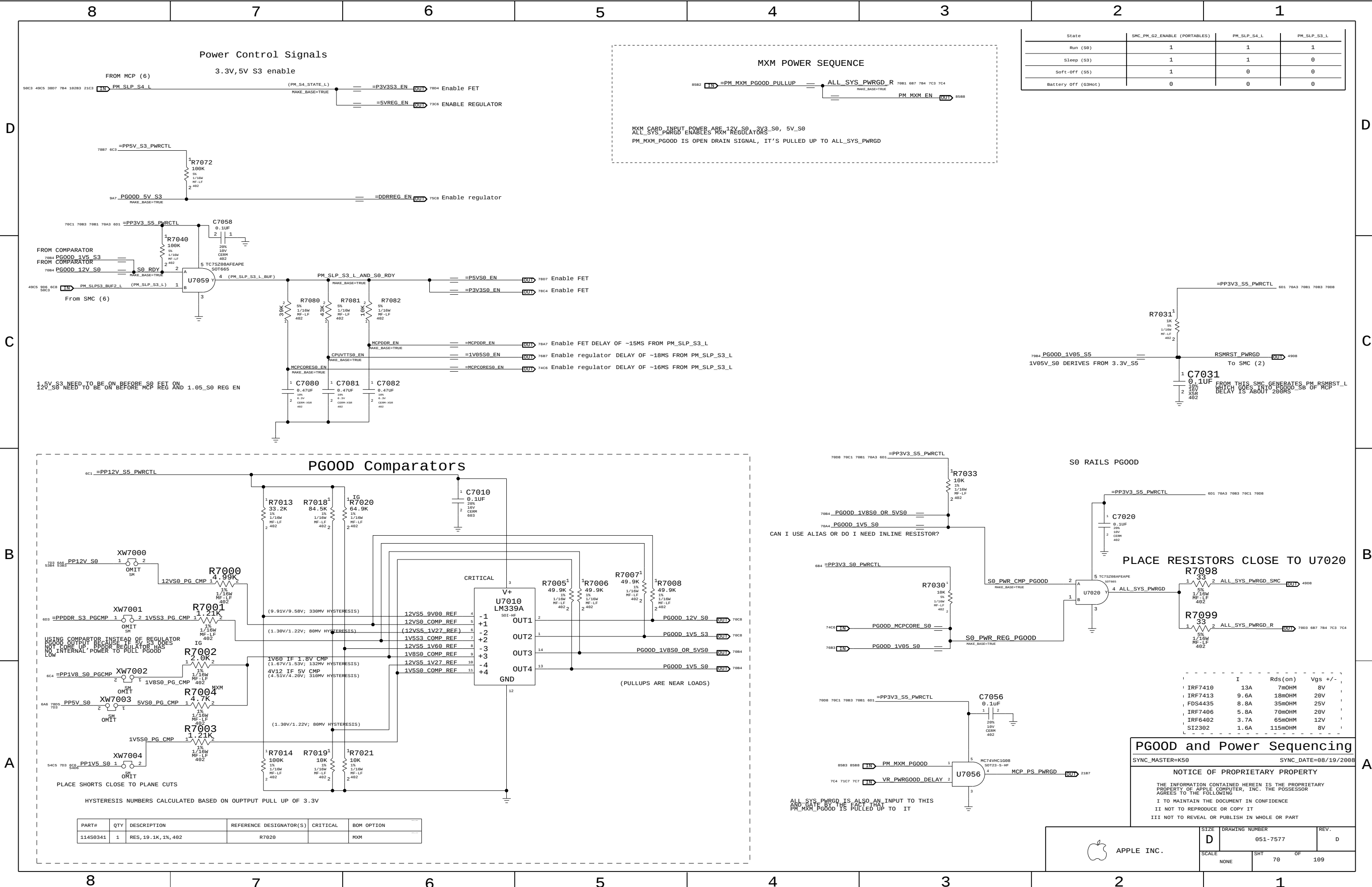






State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0





D

C

B

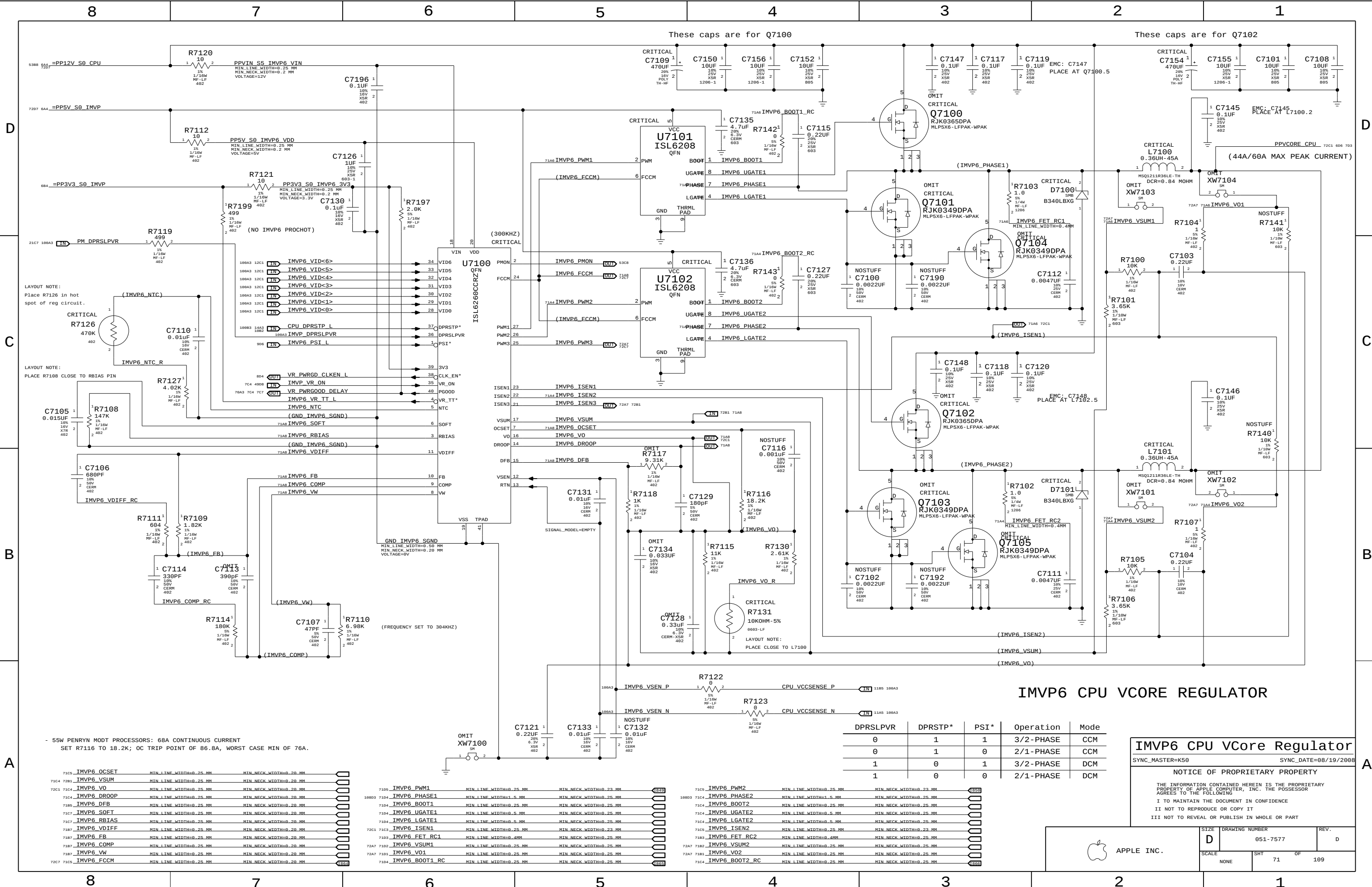
A

D

C

B

A



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=K50 SYNC_DATE=08/19/2008

NOTICE OF PROPRIETARY PROPERTY

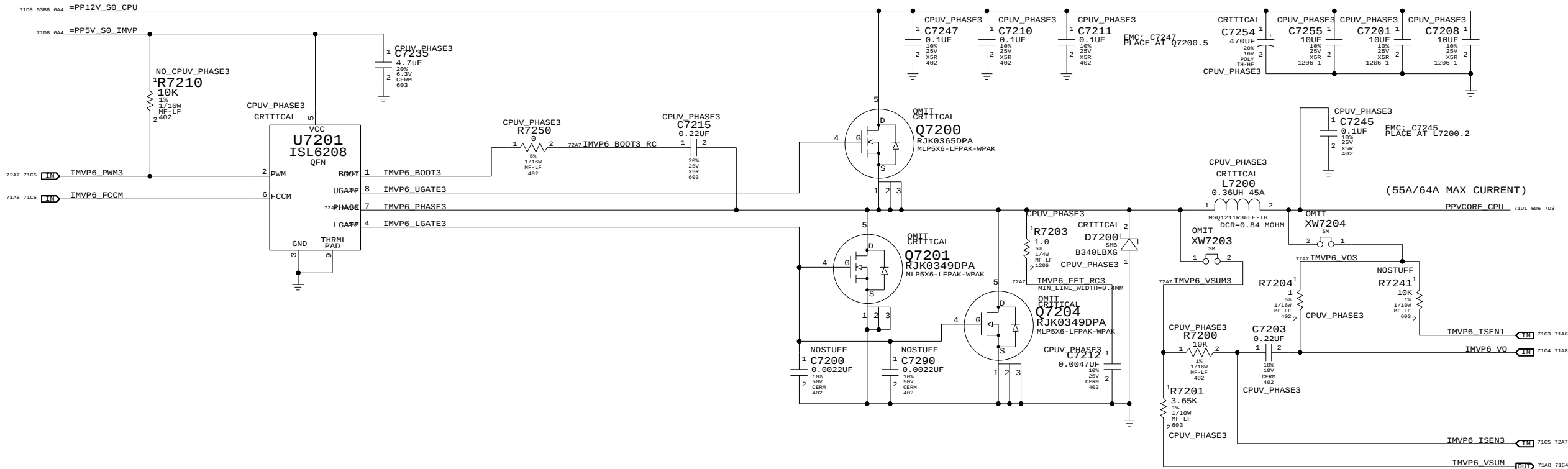
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SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	71	109

IMVP6 CPU VCORE REGULATOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	6	RENESAS BOT FET	Q7101, Q7103, Q7104, Q7105, Q7201, Q7204	RENESAS_FET
376S0733	6	TOSHIBA BOT FET	Q7101, Q7103, Q7104, Q7105, Q7201, Q7204	TOSHIBA_FET
376S0694	3	RENASAS TOP FET	Q7100, Q7102, Q7200	RENESAS_FET
376S0732	3	TOSHIBA TOP FET	Q7100, Q7102, Q7200	TOSHIBA_FET

NO TEST FOR CPU VREG, ADDED K2/K3

71A6 7101	IMVP6_V01	NO_TEST=TRUE
71A4 7201	IMVP6_V02	NO_TEST=TRUE
72A7 7202	IMVP6_V03	NO_TEST=TRUE
71A6 7102	IMVP6_VSUM1	NO_TEST=TRUE
71A4 7103	IMVP6_VSUM2	NO_TEST=TRUE
72A7 7203	IMVP6_VSUM3	NO_TEST=TRUE

72C7 71C5	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	151
10B03 72C6	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	150
72C6	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72C6	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	149
72C6	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	149
72B1 71C5	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72C3	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM	149
72A7 72C3	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72A7 72C2	IMVP6_V03	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72C5	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	150

IMVP6 3RD PHASE

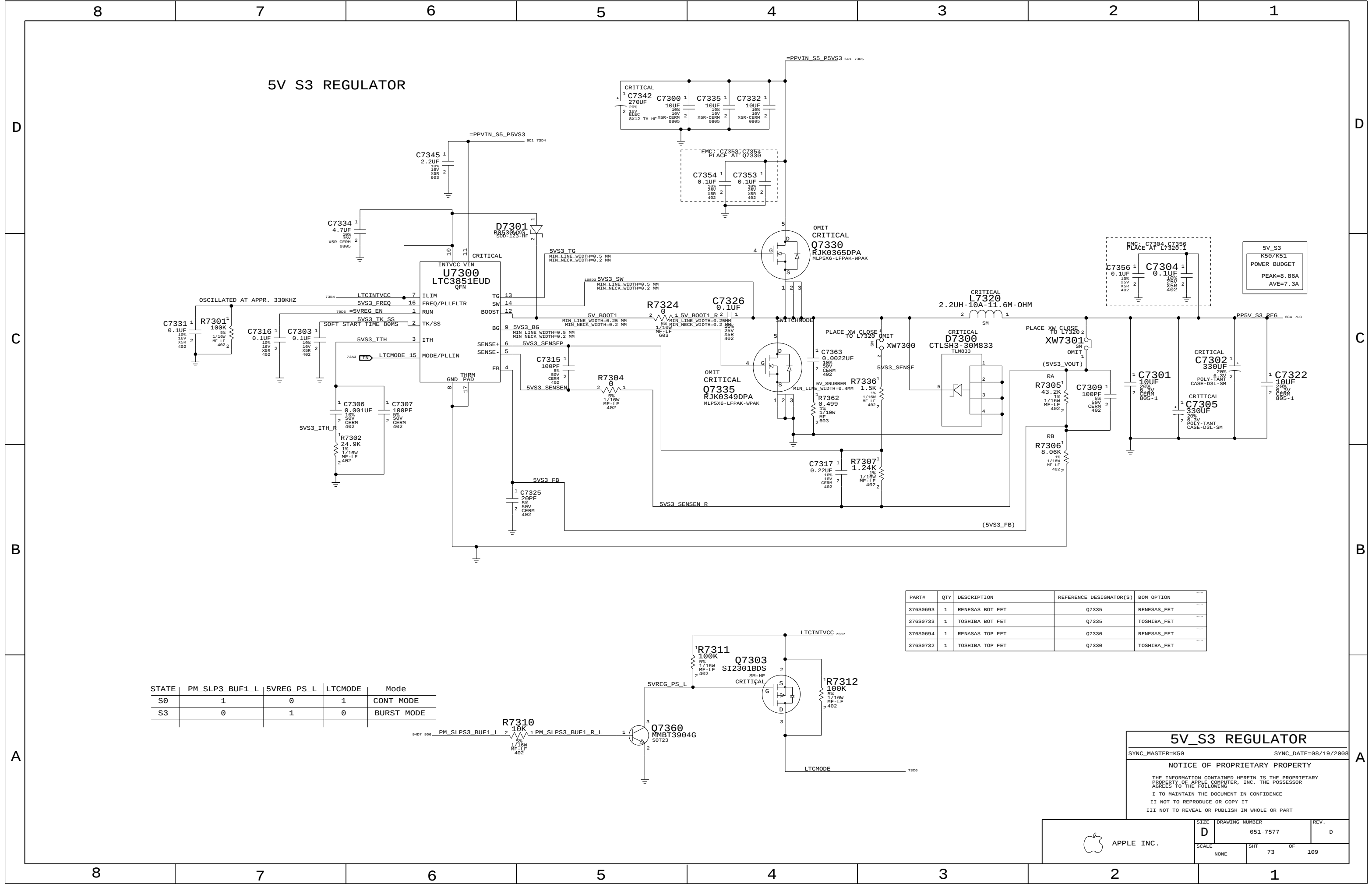
SYNC_MASTER=K50 SYNC_DATE=08/19/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	72	109



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	1	RENESAS BOT FET	Q7335	RENESAS_FET
376S0733	1	TOSHIBA BOT FET	Q7335	TOSHIBA_FET
376S0694	1	RENESAS TOP FET	Q7330	RENESAS_FET
376S0732	1	TOSHIBA TOP FET	Q7330	TOSHIBA_FET

5V_S3 REGULATOR

SYNC_MASTER=K50SYNC_DATE=08/19/2008

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SIZE D

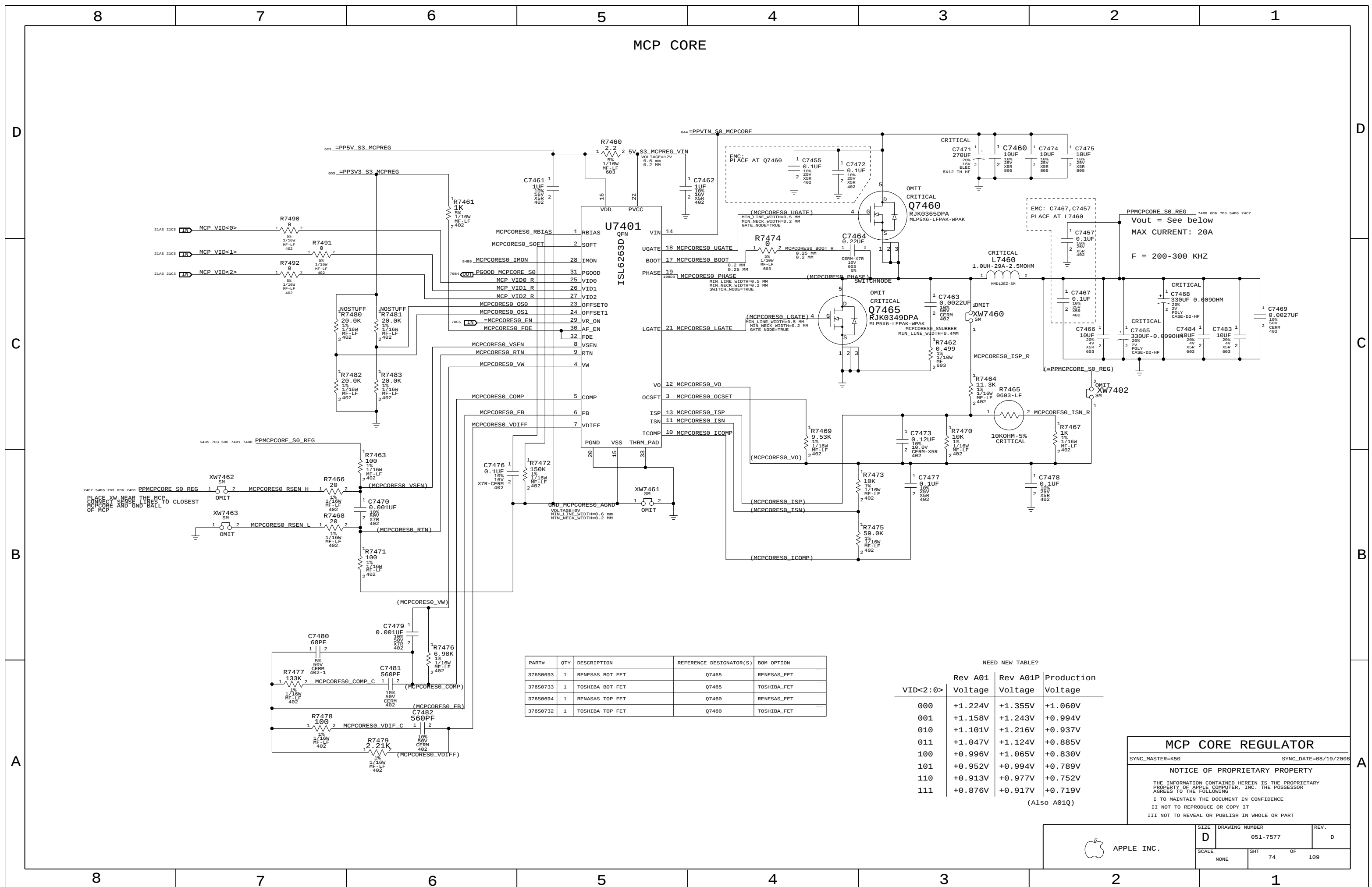
DRAWING NUMBER 051-7577

REV. D

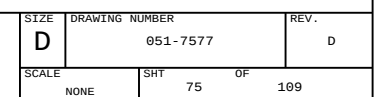
SCALE NONE

SHT 73

OF 109



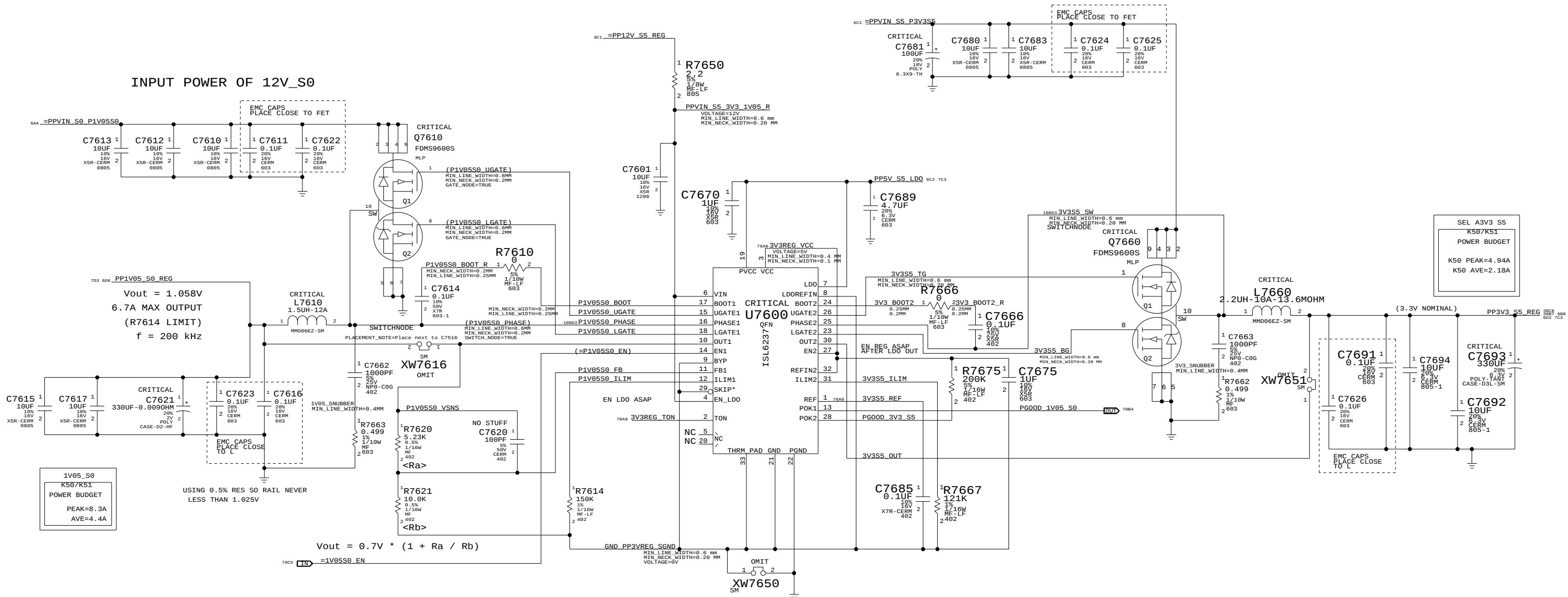
D

BA

3.3V S5 AND 1.05 S0 RAILS

INPUT POWER OF 12V_S5

INPUT POWER OF 12V_S0



EN_LDO TIED TO 12V_S5 TO EN_LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO_OUT, SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (1.05_S0) CONTROLLED SEPARATELY

1.05VS0/3.3V S5 SUPPLIES

SYNC_MASTER=K50 SYNC_DATE=08/19/2008

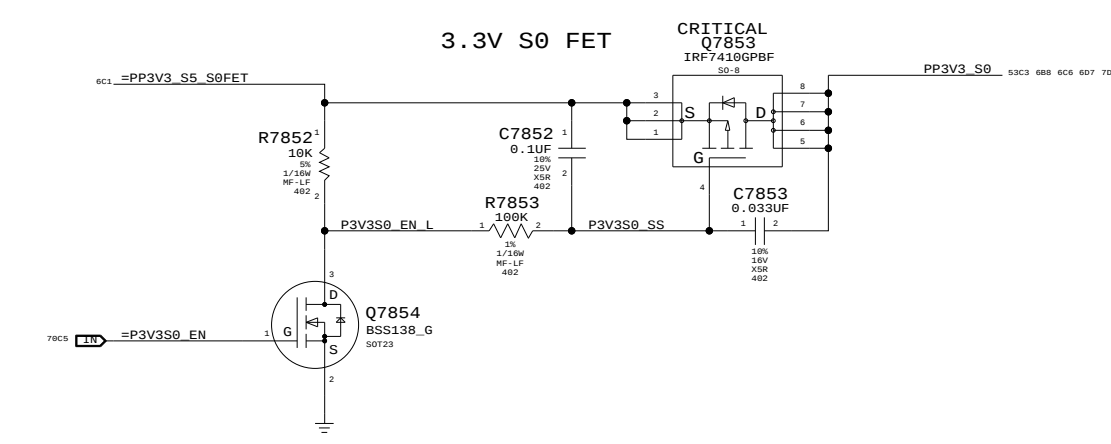
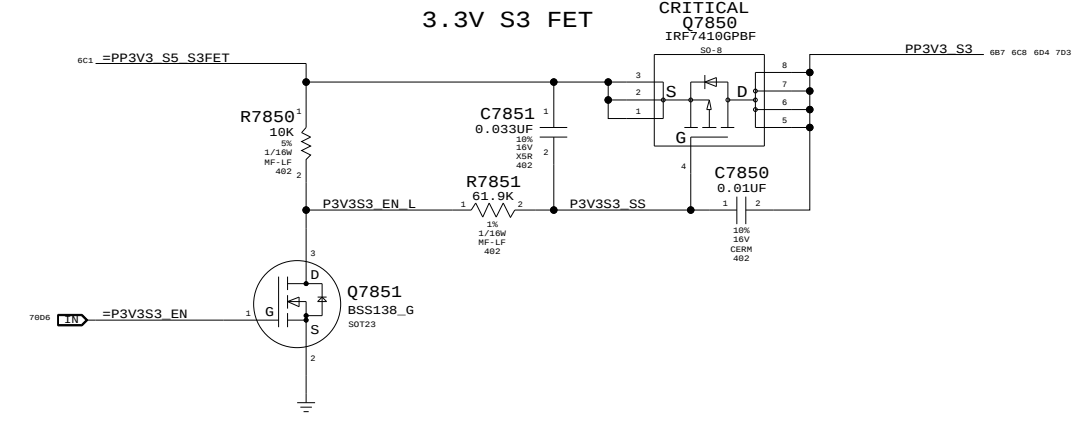
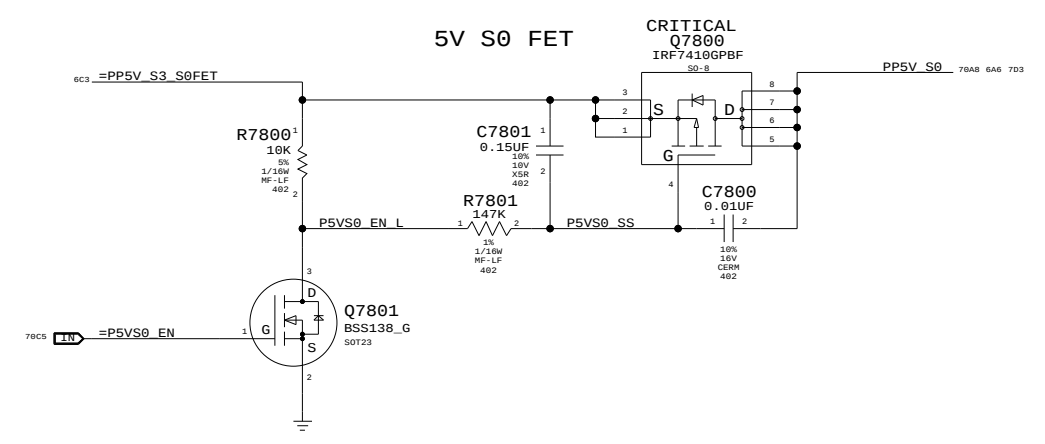
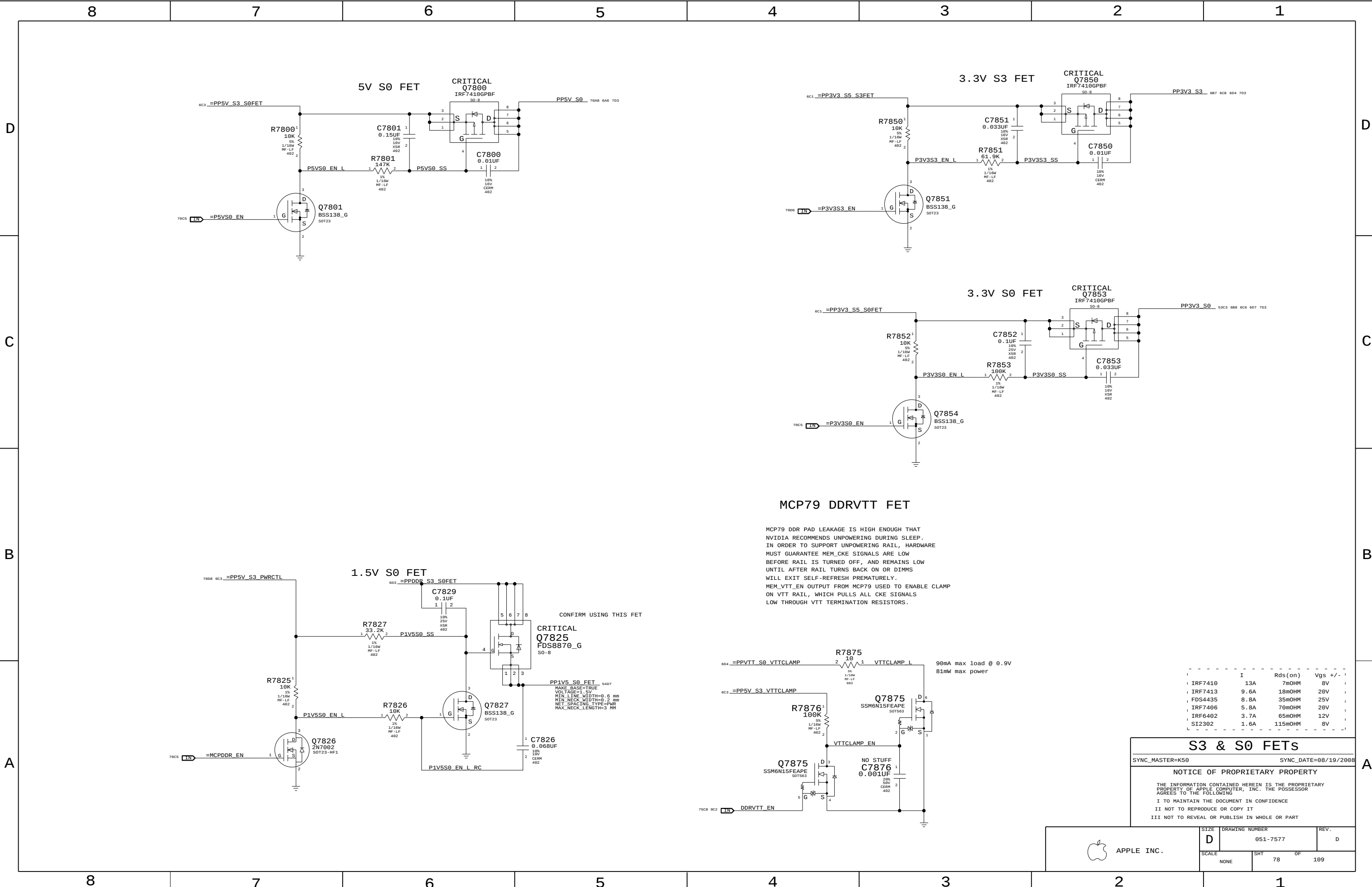
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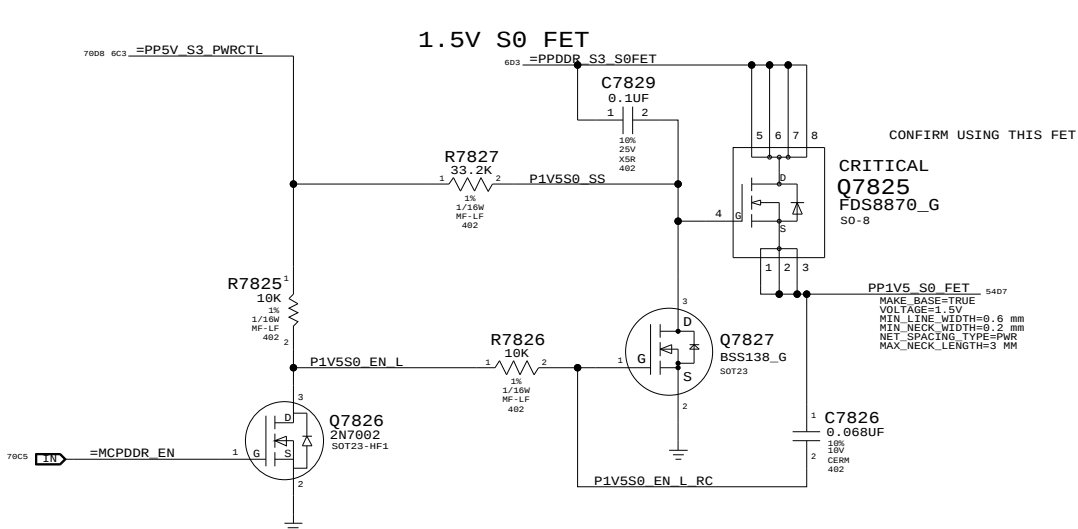
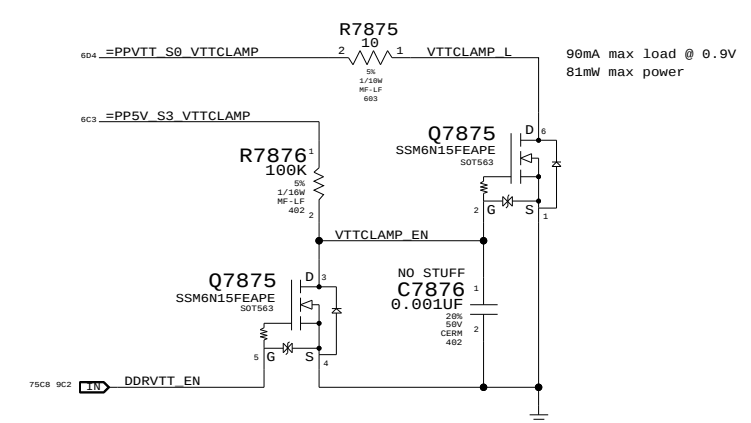
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7577	D
SCALE	SHT	OF
NONE	76	109



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL RETURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETS

SYNC_MASTER=K50 SYNC_DATE=08/19/2008

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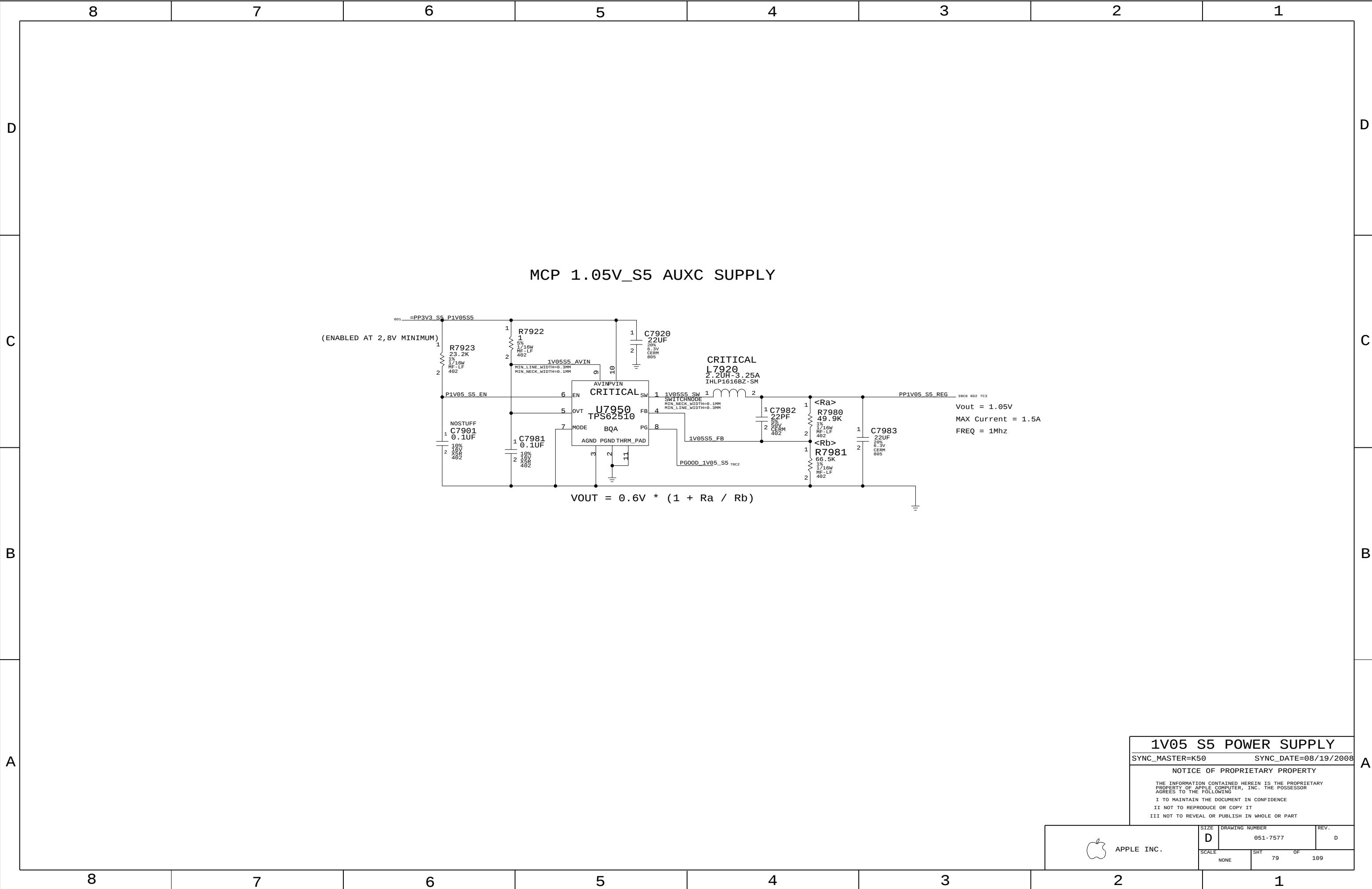
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7577	REV. D
	SCALE NONE	SHT 78 OF 109	



1V05 S5 POWER SUPPLY

SYNC_MASTER=K50

SYNC_DATE=08/19/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7577	D
SCALE		SHT	OF
NONE		79	109

Page Notes

Power aliases required by this page:

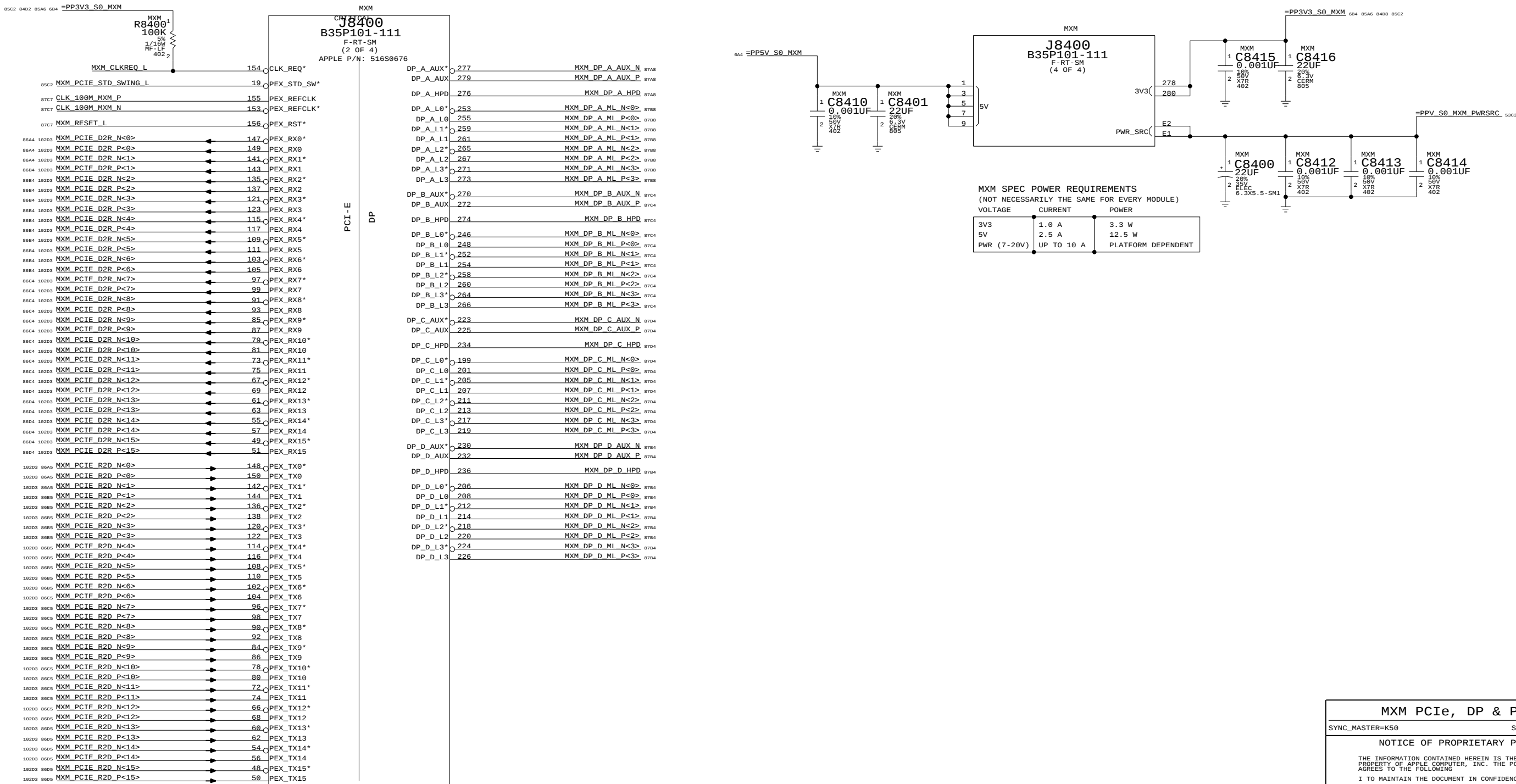
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- MXM



MXM PCIe, DP & Power

SYNC_MASTER=K50

SYNC_DATE=07/30/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7577

REV.

D

SCALE

NONE

SHT

84

OF

109

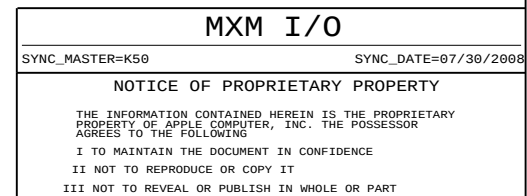
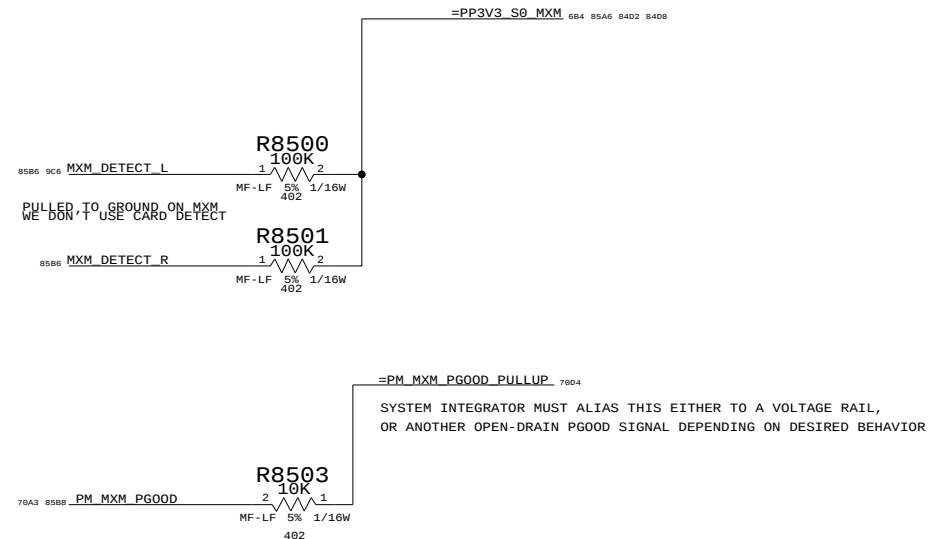
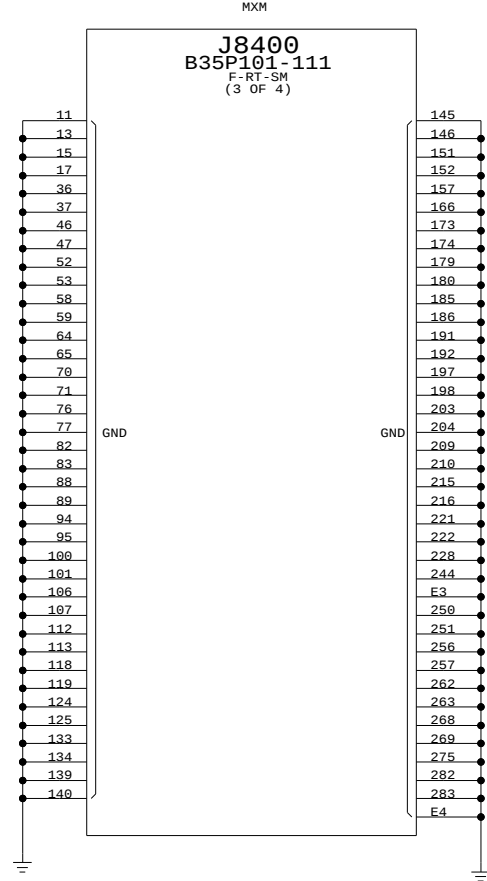
Power aliases required by this page:

- =PP3V3_S0_MXM

Signal aliases required by this page:

- =SMB_MXM_THRM_DATA - =PM_MXM_PG00D_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:



SIZE D	DRAWING NUMBER 051-7577	REV. D
SCALE NONE	SHT 85	OF 109

8	7	6	5	4	3	2	1
SLOTB MXM TX CAPS				SLOTB MXM RX CAPS			
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MXM PCIE CAPS

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

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SIZE
D

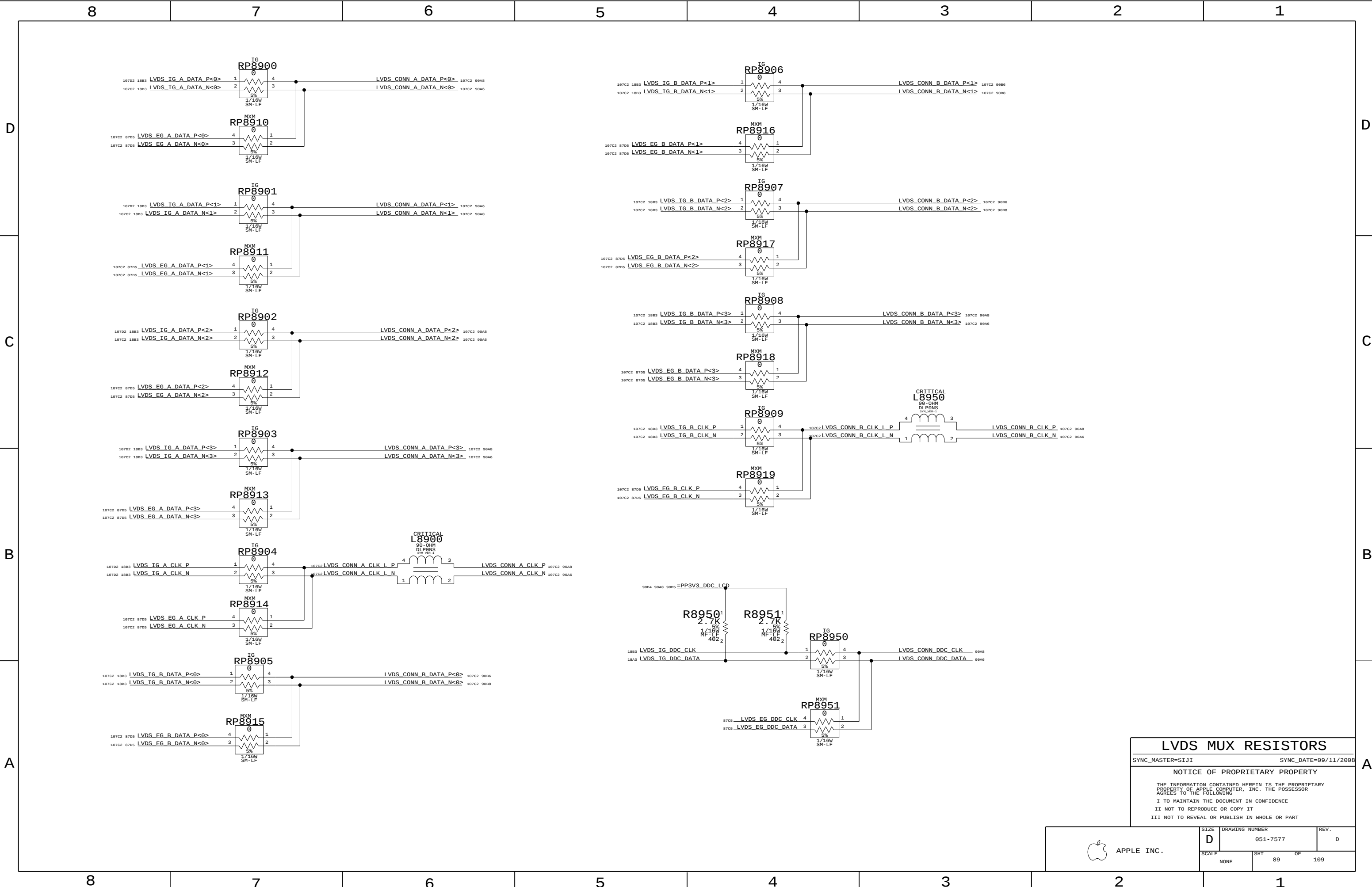
DRAWING NUMBER
051-7577

REV.
D

SCALE
NONE

SHT
86

OF
109



LVDS MUX RESISTORS

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

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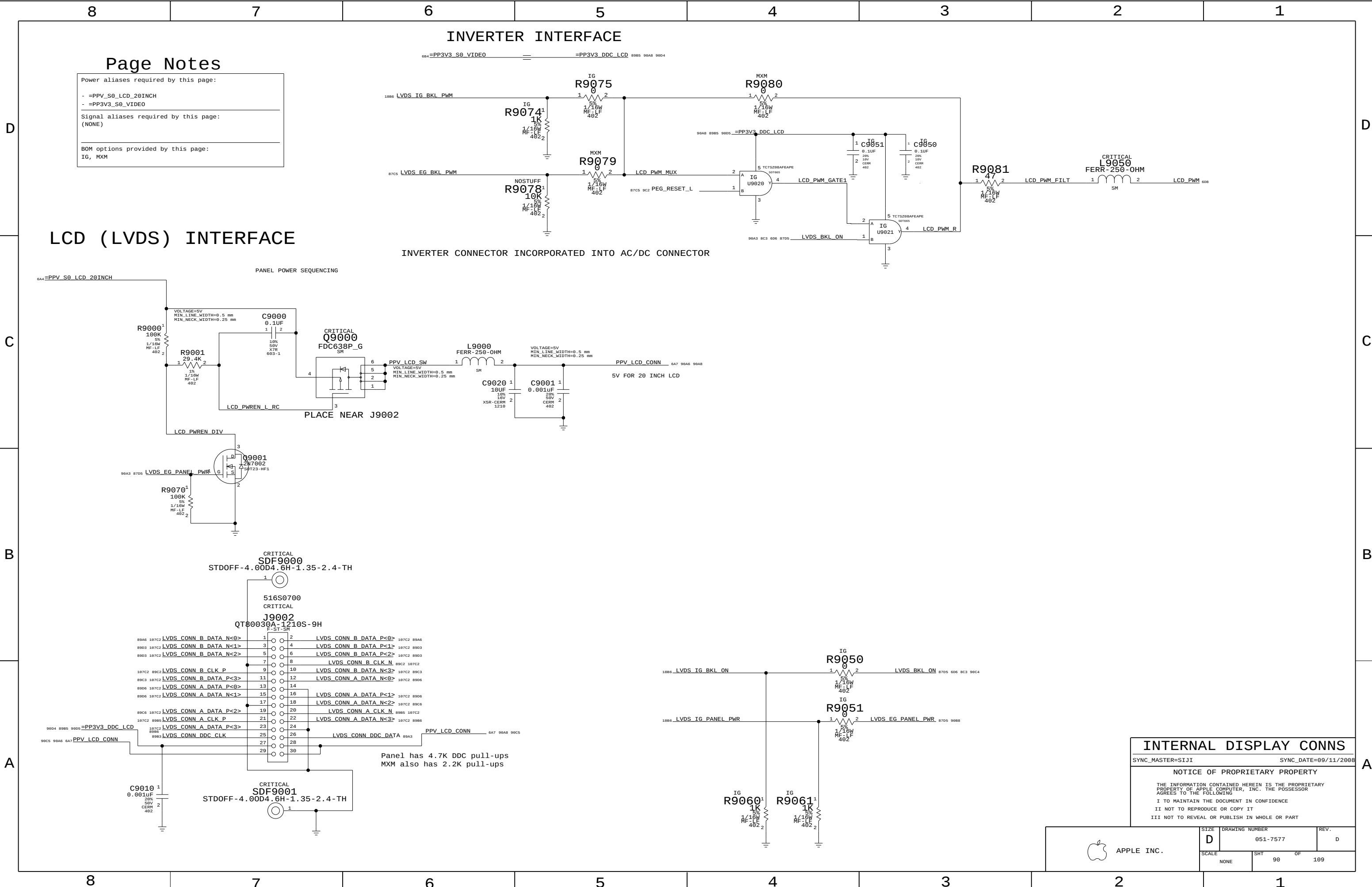
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	D	051-7577	D
SCALE		SHT	OF
NONE		89	109



Page Notes

Power aliases required by this page:

- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

IG, MXM

LCD (LVDS) INTERFACE

INVERTER INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

INTERNAL DISPLAY CONNS

SYNC_MASTER=SIJI SYNC_DATE=09/11/2008

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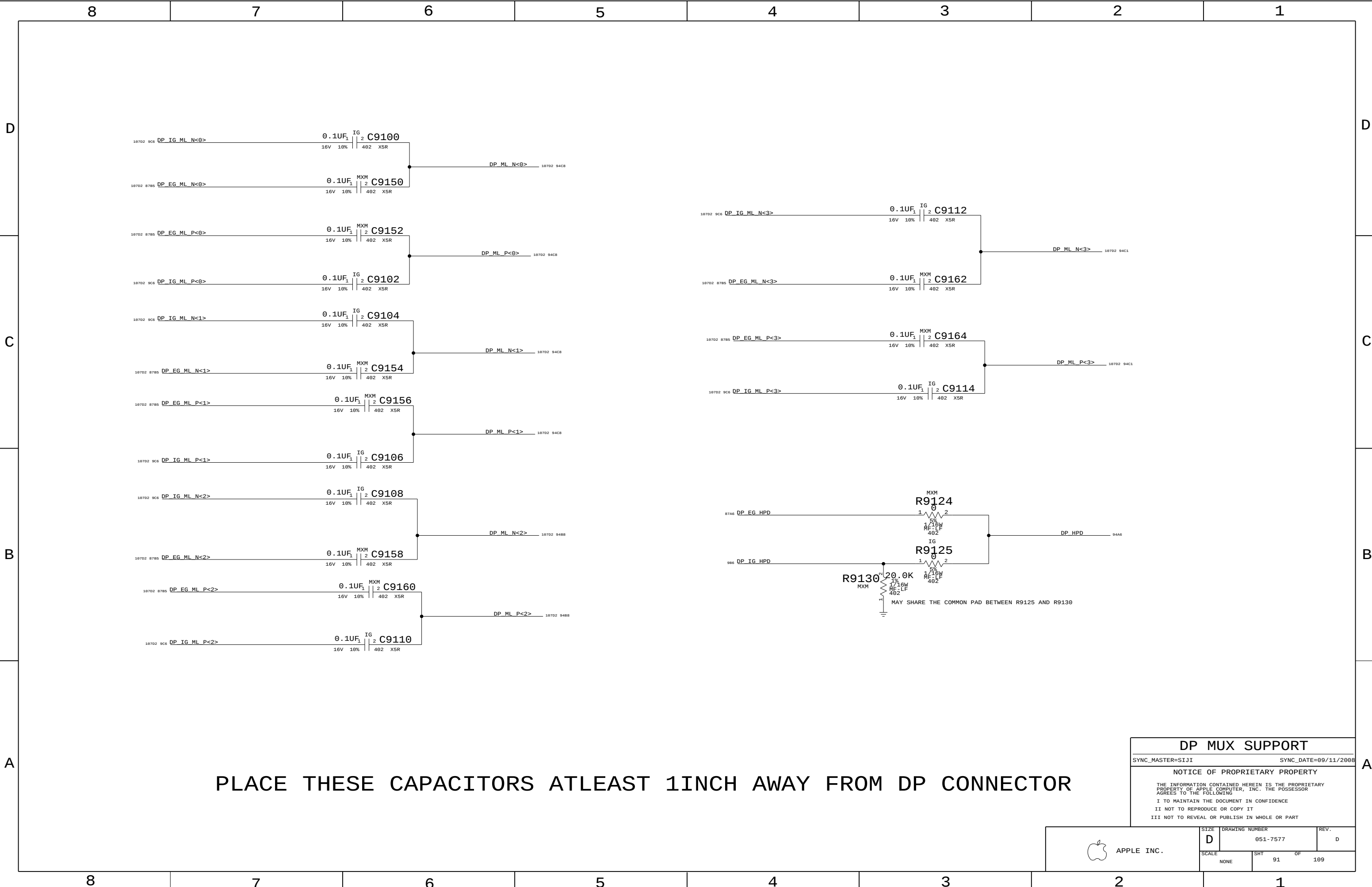
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D	051-7577	D
SCALE	SHT	OF
NONE	90	109



PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DP MUX SUPPORT

SYNC_MASTER=SIJI

SYNC_DATE=09/11/2008

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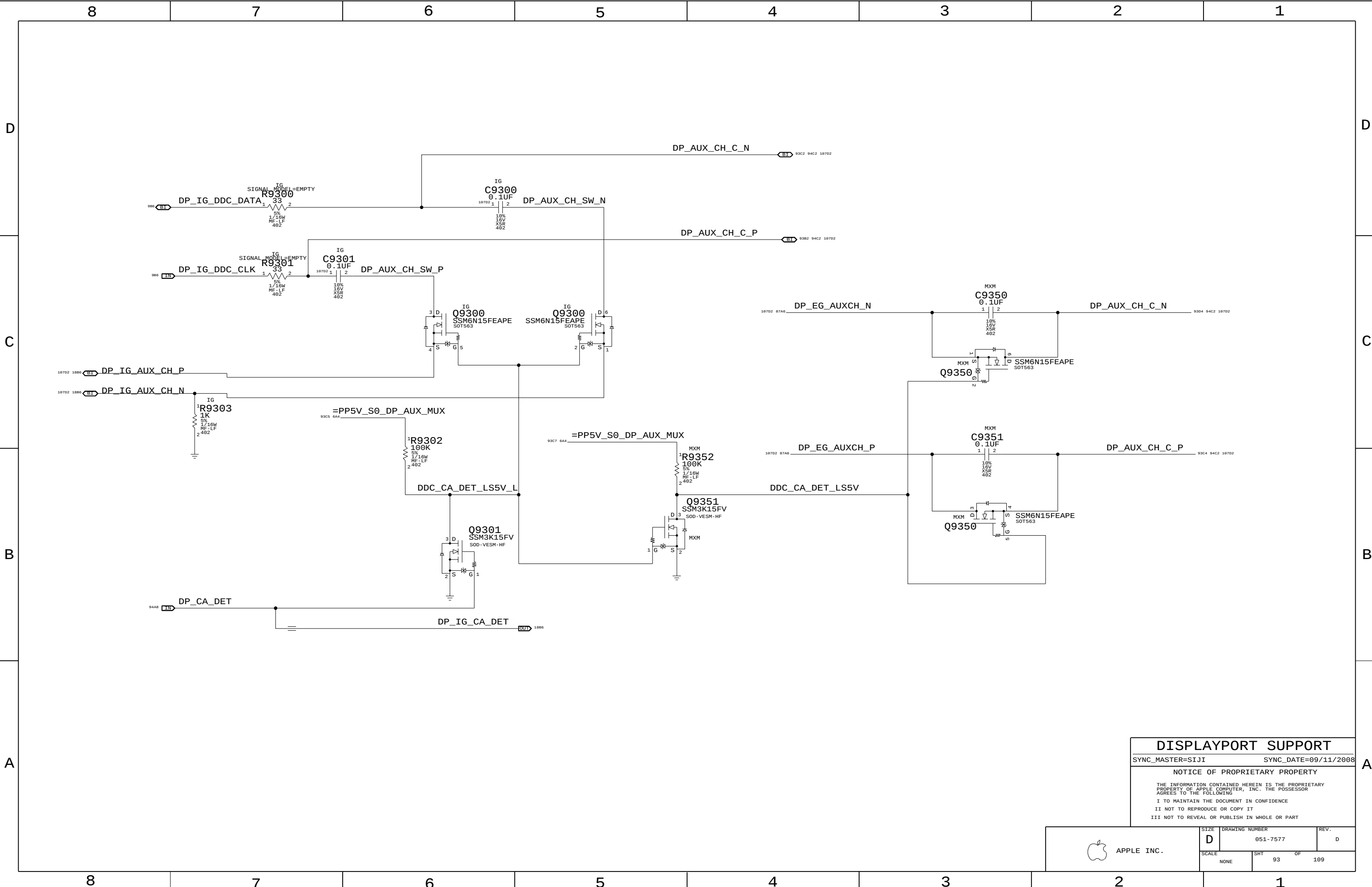
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	SCALE NONE	SHT 91	OF 109



DISPLAYPORT SUPPORT

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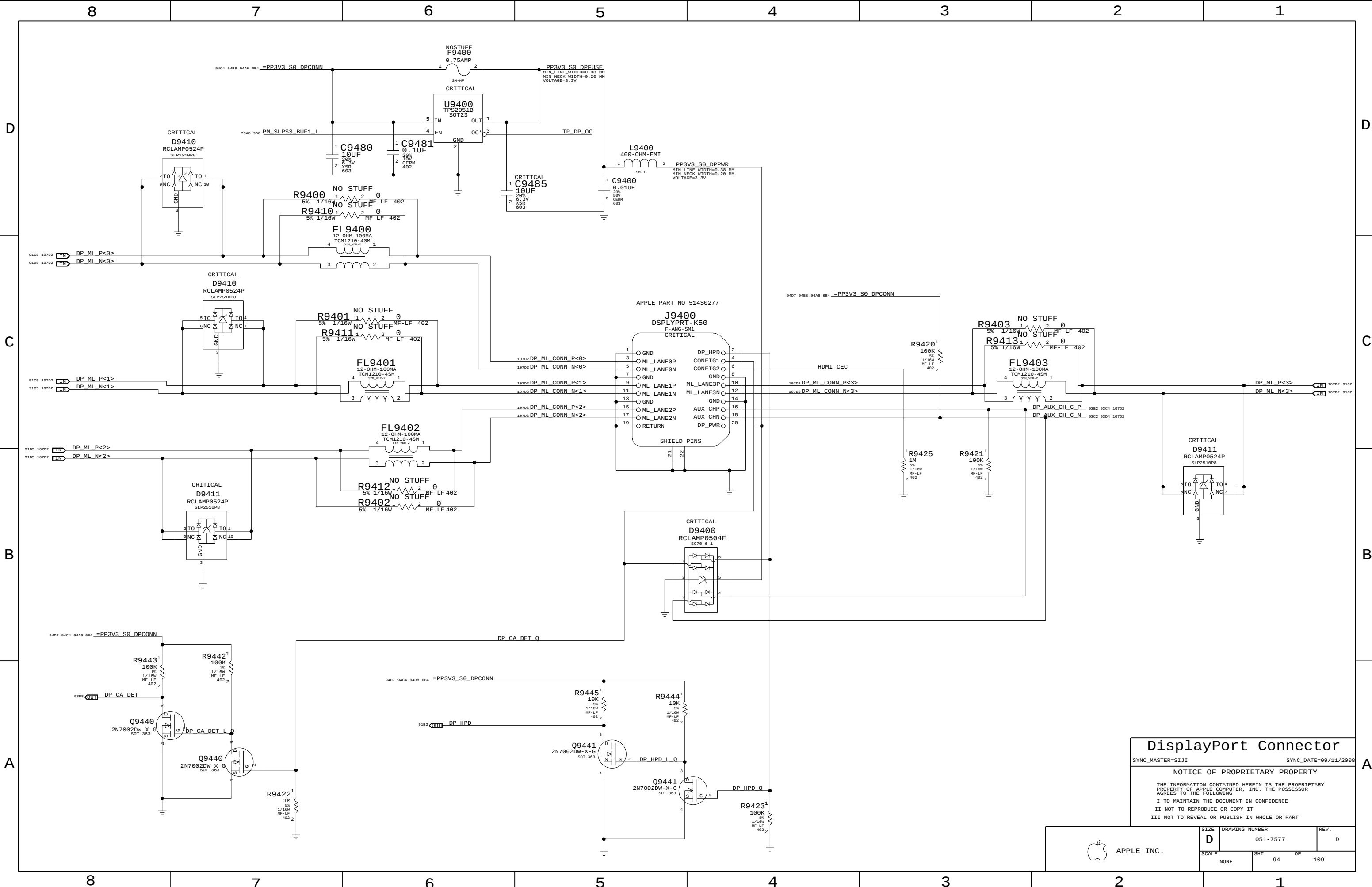
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SCALE	SHT	OF
NONE	93	109



DisplayPort Connector

SYNC_MASTER=SIJI SYNC_DATE=09/11/2008

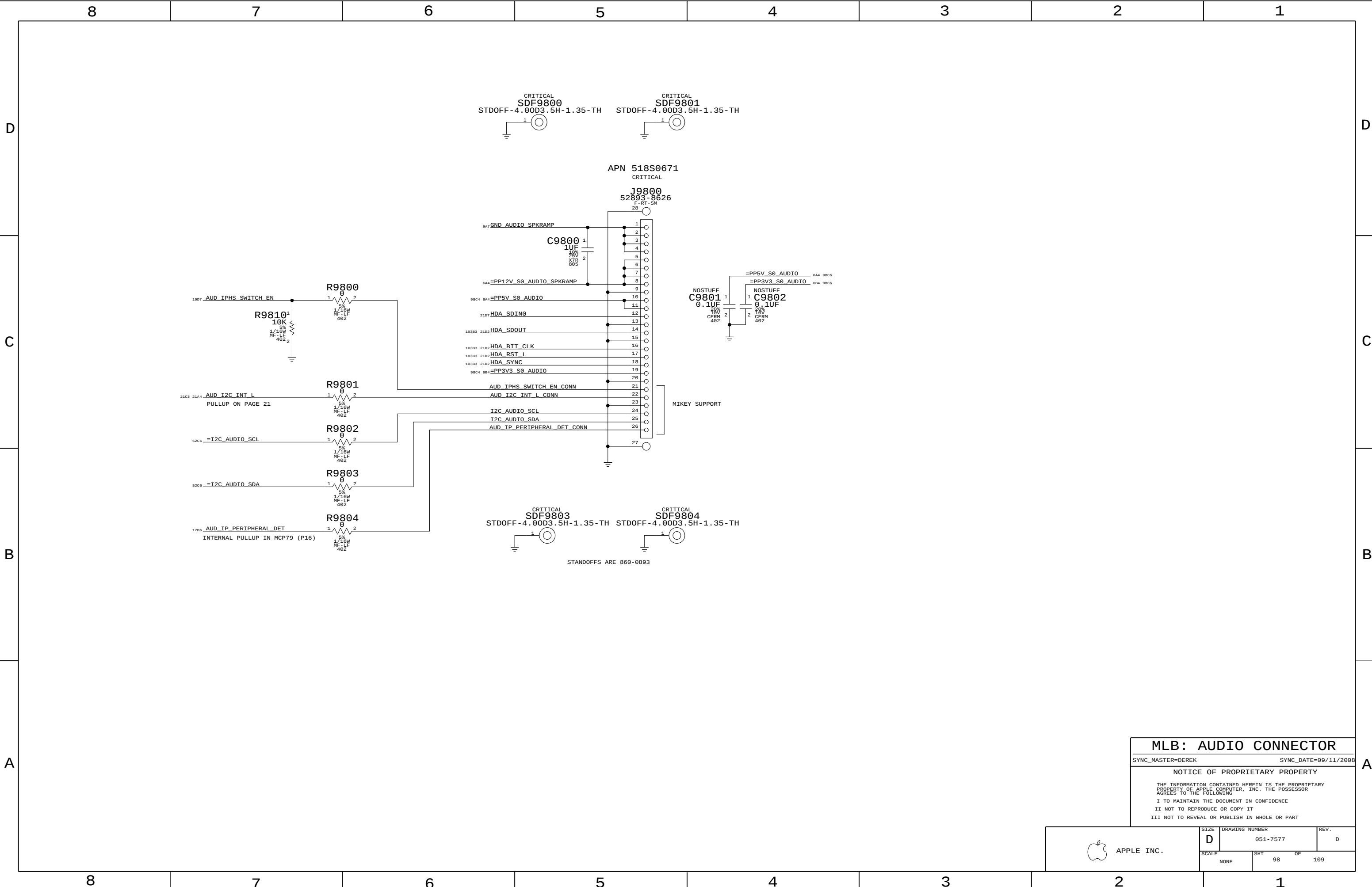
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	94	109



MLB: AUDIO CONNECTOR

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7577	REV. D
	SCALE NONE	SHT 98	OF 109

8

7

6

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2

1

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
FSB_DATA	*	=2X_DIELECTRIC	?
FSB_DSTB	*	=3X_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2X_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4X_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5X_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3X_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4X_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3X_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
CLK_FSB_1000	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CLK_FSB	*	=3X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB D L<0> 707 708 10C4 14D3
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..1> 10C4 14D3
FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB DINV L<0> 707 708 10C4 14D6
FSB_DSTB0_PP	FSB_DSTR_50S	FSB_DSTR	FSB DSTB L P<0> 707 708 10C4 14D6
FSB_DATA_GROUP1_PP	FSB_50S	FSB_DATA	FSB DSTB L N<0> 10C4 14D6
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<16> 707 708 10C4 14D3
FSB_DSTB1_PP	FSB_DSTR_50S	FSB_DSTR	FSB D L<31..17> 10B4 10C4 14C3 14D3
FSR_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<1> 10B4 14D6
FSR_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB DSTB L P<1> 707 708 10B4 14D6
FSR_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DSTB L N<1> 10B4 14D6
FSR_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB D L<40..32> 10C2 14C3
FSR_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<41> 707 708 10C2 14C3
FSR_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB D L<47..42> 10C2 14B3 14C3
FSR_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2> 707 708 10C2 14D6
FSR_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB DSTB L P<2> 10C2 14D6
FSR_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DSTB L N<2> 707 708 10C2 14D6
FSR_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB D L<58..48> 10B2 10C2 14B3
FSR_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<59> 707 708 10B2 14B3
FSR_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB D L<63..60> 10B2 14B3
FSR_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3> 707 708 10B2 14D6
FSR_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB DSTB L P<3> 10B2 14D6
FSR_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DSTB L N<3> 707 708 10B2 14D6
FSR_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<5..3> 10D8 14D6
FSR_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB A L<6> 707 708 10D8 14D6
FSR_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..7> 10D8 14C6 14D6
FSR_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB REQ L<4..0> 7C7 7C8 10D8 14B6
FSR_ADSTB0_PP	FSB_50S	FSB_ADSTB	FSB ADSTB L<0> 707 708 10D8 14B6
FSR_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<26..17> 10C8 10D8 14C6
FSR_ADDR_GROUP1_PP	FSB_50S	FSB_ADDR	FSB A L<27> 707 708 10C8 14C6
FSR_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..28> 10C8 14C6
FSR_ADDR_GROUP1_PP	FSB_50S	FSB_ADDR	FSB ADSTB L<1> 707 708 10C8 14B6
FSR_1X	FSB_50S	FSB_1X	FSB ADS L 10D6 14B6
FSB_BREQ0_L_PP	FSB_50S	FSB_1X	FSB BREQ0 L 707 10D6 14B6 23C3
FSB_1X_PP	FSB_50S	FSB_1X	FSB BRE01 L 14B6
FSB_1X	FSB_50S	FSB_1X	FSB BNR L 707 10D6 14B6
FSB_1X_PP	FSB_50S	FSB_1X	FSB BPRI L 10D6 14B3
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L 707 10D6 14B6
FSB_1X_PP	FSB_50S	FSB_1X	FSB DEFER L 10D6 14B3
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L 10D6 14B6
FSB_1X_PP	FSB_50S	FSB_1X	FSB HIT L 707 10D6 14B6
FSB_1X_PP	FSB_50S	FSB_1X	FSB HITM L 707 10D6 14B6
FSB_1X_PP	FSB_50S	FSB_1X	FSB LOCK L 707 10D6 14B6
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L 14A3 23C3 10D6 13C2
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0> 14A6 10D6
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L 14B6 10D6
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU A20M L 7D8 14A3 10C8
MCP_BSEL	CPU_50S	CPU_AGTL	MCP BSEL<2..0> 23B6 23C6
CPU_ASYNC_R	CPU_50S	CPU_8MIL	CPU FERR L 10C8 14B7
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU IGNE L 7D8 14A3 10C8
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU INIT L 7D8 14A3 10D6
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU INTR 7D8 14A3 10C8
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU NMI 7D8 14A3 10B8
CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU PROCHOT L 10C5 14B6 50B3
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD 14A3 7B4 10B2 13C7
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU SMI L 7C8 14A3 10B8
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU STPCLK L 7D8 14A3 10C8
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L 10C6 50B1 14B7
FSB_CPUSLP_P_L	CPU_50S	CPU_AGTL	FSB CPUSLP L 14A3 10B2
	CPU_50S	CPU_AGTL	CPU DPSLP L 14A3 10B2
	CPU_50S	CPU_AGTL	CPU DPRSTP L 14A3 10B2 71C7
	CPU_50S	CPU_AGTL	FSB DPWR L 7C7 14A3 10B2
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK_VML_COMP_VDD 14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK_VML_COMP_GND 14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_VCC 14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_GND 14A6
FSB_CLK_CPU_PP	CLK_FSB_1000	CLK_FSB	FSB CLK_CPU_P 7C8 14B3 10B6
FSB_CLK_ITP	CLK_FSB_1000	CLK_FSB	FSB CLK_CPU_N 7C8 14B3 7B3 10B6
FSB_CLK_ITP	CLK_FSB_1000	CLK_FSB	FSB CLK_ITP_P 14B3 7A4 13C3
FSB_CLK_MCP	CLK_FSB_1000	CLK_FSB	FSB CLK_ITP_N 14B3 7A4 13C3
	CLK_FSB_1000	CLK_FSB	FSB CLK_MCP_P 14A4
	CLK_FSB_1000	CLK_FSB	FSB CLK_MCP_N 14A4
CPU_IERR_L	CPU_50S	CPU_AGTL	CPU IERR_L 10D6
PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR 21C7 71C8
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR 71C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF 29B2 10B4
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3> 10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2> 10B3
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1> 10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0> 10B3
XDP_TDI_K50	CPU_50S	CPU_ITP	XDP TDI 13B3 7A4 10B6 10C6
XDP_TDO_K50	CPU_50S	CPU_ITP	XDP TDO 10C6 7A4 10B6 13B3
XDP_TMS_K50	CPU_50S	CPU_ITP	XDP TMS 13B3 7A4 10B6 10C6
XDP_TCK_K50	CPU_50S	CPU_ITP	XDP TCK 13B6 7A4 10A6 10C6
XDP_TRST_L_K50	CPU_50S	CPU_ITP	XDP TRST_L 13B3 7A4 10A6 10C6
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0> 10C6 13C6 7B4
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5> 10C5 13C6 7B4
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST_L 7A4 13C4
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0> 12C1 71C7
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P 11B5 71A3
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N 11A5 71A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P 71A5
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N 71A5

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FSB 4X Signal Groups

FSB 2X Signals

FSB 1X Signals

D

C

B

A

CPU/FSB Constraints

SYNC_MASTER=AARON SYNC_DATE=03/27/2008

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DRAWING NUMBER

051-7577

REV.

D

SCALE

NONE

SHT

100

OF

109

PCI-Express

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERM	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_900	PCIE	PEG R2D C P<15..0>
	PCIE_900	PCIE	PEG R2D C N<15..0>
	PCIE_900	PCIE	PEG D2R P<15..0>
	PCIE_900	PCIE	PEG D2R N<15..0>
PEG_R2D	PCIE_900	PCIE	MXM PCIE R2D P<15..0>
	PCIE_900	PCIE	MXM PCIE R2D N<15..0>
PEG_D2R_MXM3	PCIE_900	PCIE	MXM PCIE D2R P<7..0>
PEG_D2R_MXM3_PP	PCIE_900	PCIE	MXM PCIE D2R P<8>
PEG_D2R_MXM3	PCIE_900	PCIE	MXM PCIE D2R P<15..9>
	PCIE_900	PCIE	MXM PCIE D2R N<15..0>
	PCIE_900	PCIE	PCIE MINI R2D P
	PCIE_900	PCIE	PCIE MINI R2D N
PCIE_MINI_R2D	PCIE_900	PCIE	PCIE MINI R2D C P
	PCIE_900	PCIE	PCIE MINI R2D C N
PCIE_MINI_D2R_PP	PCIE_900	PCIE	PCIE MINI D2R P
	PCIE_900	PCIE	PCIE MINI D2R N
	PCIE_900	PCIE	PCIE FW_R2D P
	PCIE_900	PCIE	PCIE FW_R2D N
PCIE_FW_R2D_PP	PCIE_900	PCIE	PCIE FW_R2D C P
	PCIE_900	PCIE	PCIE FW_R2D C N
PCIE_FW_D2R_PP	PCIE_900	PCIE	PCIE FW_D2R P
	PCIE_900	PCIE	PCIE FW_D2R N
	PCIE_900	PCIE	PCIE FW_D2R C P
	PCIE_900	PCIE	PCIE FW_D2R C N
MCP_PER_REFCLK	CLK_PCIE_1080	CLK_PCIE	GPU_CLK100M_PCIE_P
	CLK_PCIE_1080	CLK_PCIE	GPU_CLK100M_PCIE_N
MCP_PE1_REFCLK	CLK_PCIE_1080	CLK_PCIE	PCIE_CLK100M_MINI_P
	CLK_PCIE_1080	CLK_PCIE	PCIE_CLK100M_MINI_N
MCP_PE2_REFCLK_PP	CLK_PCIE_1080	CLK_PCIE	PCIE_CLK100M_FW_P
	CLK_PCIE_1080	CLK_PCIE	PCIE_CLK100M_FW_N
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE
MCP_PEX_CLK_COMP	MCP_SBS	MCP_PEX_COMP	MCP_PEX_CLK_COMP
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET
MCP_IFPAB_VPROBE	MCP_SBS	MCP_PEX_COMP	MCP_IFPAB_VPROBE
SATA_HDD_R2D	SATA_1080	SATA	SATA_HDD_R2D C P
	SATA_1080	SATA	SATA_HDD_R2D C N
	SATA_1080	SATA	SATA_HDD_R2D P
	SATA_1080	SATA	SATA_HDD_R2D N
SATA_HDD_D2R_PP	SATA_1080	SATA	SATA_HDD_D2R P
	SATA_1080	SATA	SATA_HDD_D2R N
	SATA_1080	SATA	SATA_HDD_D2R C P
	SATA_1080	SATA	SATA_HDD_D2R C N
SATA_ODD_R2D	SATA_1080	SATA	SATA_ODD_R2D C P
	SATA_1080	SATA	SATA_ODD_R2D C N
	SATA_1080	SATA	SATA_ODD_R2D P
	SATA_1080	SATA	SATA_ODD_R2D N
SATA_ODD_D2R_PP	SATA_1080	SATA	SATA_ODD_D2R P
	SATA_1080	SATA	SATA_ODD_D2R N
	SATA_1080	SATA	SATA_ODD_D2R C P
	SATA_1080	SATA	SATA_ODD_D2R C N
MCP_SATA_TERMPP	MCP_SBS	SATA_TERMPP	MCP_SATA_TERMPP
PM_SLP_S3_L			PM_SLP_S3_L
PM_SLP_S4_L			PM_SLP_S4_L

MCP Constraints 1	
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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MCP_USB_RBIA5	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	783 1902 1907
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	783 1902 1907
PCI_CLK33M_MCP	CLK_PCT_55S	CLK_PCT	PCI_CLK33M_MCP_R	19C5
LPC_AD	LPC_55S	LPC	PCI_CLK33M_MCP	19C5
LPC_AD_2PP	LPC_55S	LPC	LPC_AD<0>	1983 49C8 51D5 7D4
LPC_AD	LPC_55S	LPC	LPC_AD<1>	788 7D6 1983 49C8 51D5 7D4
LPC_AD	LPC_55S	LPC	LPC_AD<3..2>	1983 49C8 51D4 7D4
LPC_AD	LPC_55S	LPC	LPC_AD_R<3..0>	1985
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19C3 7D4 49C8 51D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_PU	51C2
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_R_L	19C5 51C1
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19C3 9D4
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	1983 984
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	982 49C8
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	982 7D4 51D4
MCP_SUS_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	2183 984
MCP_SUS_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	982 49C5
MCP_USB_RBIA5	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	29C4
USB_EXT	USB_90D	USB	USB_EXT_A_P	29D3 46A7
USB_EXT	USB_90D	USB	USB_EXT_A_N	29D3 46A7
USB_EXT	USB_90D	USB	USB_PORT0_P	46A5
USB_EXT	USB_90D	USB	USB_PORT0_N	46A5
USB_EXT	USB_90D	USB	USB_EXTB_P	29C3 46B6
USB_EXT	USB_90D	USB	USB_EXTB_N	29C3 46B6
USB_EXT	USB_90D	USB	USB_PORT1_P	46B5
USB_EXT	USB_90D	USB	USB_PORT1_N	46B5
USB_EXT	USB_90D	USB	USB_EXTC_P	29C3 46B3
USB_EXT	USB_90D	USB	USB_EXTC_N	29C3 46B3
USB_EXT	USB_90D	USB	USB_PORT2_P	46B2
USB_EXT	USB_90D	USB	USB_PORT2_N	46B2
USB_EXT_MUXED	USB_90D	USB	USB_EXTD_P	29D3 46D5
USB_EXT_MUXED	USB_90D	USB	USB_EXTD_N	29D3 46D5
USB_EXT_MUXED	USB_90D	USB	USB_D_MUXED_P	46D4
USB_EXT_MUXED	USB_90D	USB	USB_D_MUXED_N	46D4
USB_MINI	USB_90D	USB	USB_PORT3_P	46D3
USB_MINI	USB_90D	USB	USB_PORT3_N	46D3
USB_MINI	USB_90D	USB	USB_MINI_P	29D3 34B3
USB_MINI	USB_90D	USB	USB_MINI_N	29D3 34B3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	788 29D3 47B7
USB_CAMERA	USB_90D	USB	USB_CAMERA_N	788 29D3 47B7
USB_CAMERA	USB_90D	USB	USB_CAMERA_L_P	47B6
USB_CAMERA	USB_90D	USB	USB_CAMERA_L_N	47B6
USB_BT_PP	USB_90D	USB	USB_BT_P	788 29D3 47D4
USB_BT_PP	USB_90D	USB	USB_BT_N	788 29C3 47D4
USB_IR	USB_90D	USB	USB_IR_P	29D3 47B4
USB_IR	USB_90D	USB	USB_IR_N	29D3 47B4
USB_IR	USB_90D	USB	USB_IR_L_P	47B3
USB_IR	USB_90D	USB	USB_IR_L_N	47B3
SPI_CLK	MCP_55S	SPI	SPI_CLK_R	788 2183 51A6 61C6
SPI_CLK	MCP_55S	SPI	SPI_CLK	61C5
SPI_MOSI	MCP_55S	SPI	SPI_MOSI_R	2183 51A6 61C2
SPI_MOSI	MCP_55S	SPI	SPI_MOSI	61C4
SPI_MISO	MCP_55S	SPI	SPI_MISO	788 51A6 61B2 2183
SPI_MISO	MCP_55S	SPI	SPI_MISO_R	61B4
SPI_CS0	MCP_55S	SPI	SPI_CS0_R_L	2183 51C6
SPI_CS0	MCP_55S	SPI	SPI_CS0_L	51C7
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	21D2 98C6
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK_R	21D4 21A7
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21D2 98C6
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21D4 21A7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21D2 98C6
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT_R	21D4 21A7
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21D2 98C6
HDA_SYNC	HDA_55S	HDA	HDA_SYNC_R	21D4 21A7

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MCP Constraints 2

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FireWire Constraints

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D	051-7577	D
SCALE	SHT 105 OF 109	
NONE		

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_OV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mills. Pairs should be within 100 mills of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONNECT_SET		PHYSICAL		NET TYPE		SPACING					
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP EG_ML_P<3..0>	8785	9187	91C4	91C8			
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP IG_ML_P<3..0>	9C6	9187	9188	91C4	91C8		
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP EG_ML_N<3..0>	8785	9188	91C4	91C8	91D8		
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP IG_ML_N<3..0>	9C6	9188	91C8	91D4	91D8		
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP_ML_P<3..0>	9185	91C2	91C5	9488	94C1	94C8	
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP_ML_N<3..0>	9185	91C2	91C5	91D5	9488	94C1	94C8
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP_ML_CONN_P<3..0>	94C4	94C5					
	DP_ML_MXMX3	DP_1000	DISPLAYPORT	DP_ML_CONN_N<3..0>	94C4	94C5					
	DP_IG_AUX_CH	DP_1000	DISPLAYPORT	DP_IG_AUX_CH_P	1886	93C8					
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_IG_AUX_CH_N	1886	93C8					
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH_SW_P	93C6						
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH_SW_N	93D5						
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH_C_P	93B2	93C4	94C2				
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP_AUX_CH_C_N	93C2	93C4	94C2				
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP EG_AUXCH_P	87A6	93B4					
	DP_AUX_CH	DP_1000	DISPLAYPORT	DP EG_AUXCH_N	87A6	93C4					
	LVDS_A_CLK_MXMX3	LVDS_1000	LVDS	LVDS_IG_A_CLK_P	18B3	89B8					
	LVDS_A_CLK_MXMX3	LVDS_1000	LVDS	LVDS_IG_A_CLK_N	18B3	89B8					
	LVDS_A_DATA_MXMX3	LVDS_1000	LVDS	LVDS_IG_A_DATA_P<3..0>	18B3	89B8	89C8	89D8			
	LVDS_A_DATA_MXMX3	LVDS_1000	LVDS	LVDS_IG_A_DATA_N<3..0>	18B3	89B8	89C8	89D8			
	LVDS_B_CLK_MXMX3	LVDS_1000	LVDS	LVDS_IG_B_CLK_P	18B3	89C5					
	LVDS_B_CLK_MXMX3	LVDS_1000	LVDS	LVDS_IG_B_CLK_N	18B3	89C5					
	LVDS_B_DATA_MXMX3	LVDS_1000	LVDS	LVDS_IG_B_DATA_P<3..0>	18B3	89A8	89C5	89D5			
	LVDS_B_DATA_MXMX3	LVDS_1000	LVDS	LVDS_IG_B_DATA_N<3..0>	18B3	89A8	89C5	89D5			
	LVDS_A_CLK_MXMX3	LVDS_1000	LVDS	LVDS EG_A_CLK_P	87D5	89B8					
	LVDS_A_CLK_MXMX3	LVDS_1000	LVDS	LVDS EG_A_CLK_N	87D5	89B8					
	LVDS_A_DATA_MXMX3	LVDS_1000	LVDS	LVDS EG_A_DATA_P<3..0>	87D5	89B8	89C8	89D8			
	LVDS_A_DATA_MXMX3	LVDS_1000	LVDS	LVDS EG_A_DATA_N<3..0>	87D5	89B8	89C8	89D8			
	LVDS_B_CLK_MXMX3	LVDS_1000	LVDS	LVDS EG_B_CLK_P	87D5	89B5					
	LVDS_B_CLK_MXMX3	LVDS_1000	LVDS	LVDS EG_B_CLK_N	87D5	89B5					
	LVDS_B_DATA_MXMX3	LVDS_1000	LVDS	LVDS EG_B_DATA_P<3..0>	87D5	89A8	89C5	89D5			
	LVDS_B_DATA_MXMX3	LVDS_1000	LVDS	LVDS EG_B_DATA_N<3..0>	87D5	89A8	89C5	89D5			
	LVDS_CONN_A_CLK_P	LVDS_1000	LVDS	LVDS_CONN_A_CLK_P	89B5	90A8					
	LVDS_CONN_A_CLK_N	LVDS_1000	LVDS	LVDS_CONN_A_CLK_N	89B5	90A6					
	LVDS_CONN_A_DATA_P<3..0>	LVDS_1000	LVDS	LVDS_CONN_A_DATA_P<3..0>	89B6	89C6	89D6	90A6	90A8		
	LVDS_CONN_A_DATA_N<3..0>	LVDS_1000	LVDS	LVDS_CONN_A_DATA_N<3..0>	89B6	89C6	89D6	90A6	90A8		
	LVDS_CONN_B_CLK_P	LVDS_1000	LVDS	LVDS_CONN_B_CLK_P	89C2	90A8					
	LVDS_CONN_B_CLK_N	LVDS_1000	LVDS	LVDS_CONN_B_CLK_N	89C2	90A6					
	LVDS_CONN_B_DATA_P<3..0>	LVDS_1000	LVDS	LVDS_CONN_B_DATA_P<3..0>	89A6	89C3	89D3	90A8	90B6		
	LVDS_CONN_B_DATA_N<3..0>	LVDS_1000	LVDS	LVDS_CONN_B_DATA_N<3..0>	89A6	89C3	89D3	90A6	90B8		
	LVDS_CONN_A_CLK_L_P	LVDS_1000	LVDS	LVDS_CONN_A_CLK_L_P	89B7						
	LVDS_CONN_A_CLK_L_N	LVDS_1000	LVDS	LVDS_CONN_A_CLK_L_N	89B7						
	LVDS_CONN_B_CLK_L_P	LVDS_1000	LVDS	LVDS_CONN_B_CLK_L_P	89C4						
	LVDS_CONN_B_CLK_L_N	LVDS_1000	LVDS	LVDS_CONN_B_CLK_L_N	89C4						

GRAPHICS CONSTRAINTS

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	600 MIL_OVERRIDE	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	600 MIL_OVERRIDE	VERRIDE	VERRIDE
MEM_780_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	600 MIL_OVERRIDE	VERRIDE	VERRIDE
PCIE_90D_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
USB_90D_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	VERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_MII_COMP_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_USB_RBIAS_OVERRIDE	TOP_OVERRIDE	VERRIDE	VERRIDE	0.1 MM_OVERRIDE	500 MIL_OVERRIDE	VERRIDE	VERRIDE
MCP_DV_COMP_OVERRIDE	*_OVERRIDE	VERRIDE	VERRIDE	0.25 MM_OVERRIDE	250 MIL_OVERRIDE	VERRIDE	VERRIDE
CPU_27P4S_OVERRIDE	BOTTOM_OVERRIDE	VERRIDE	VERRIDE	0.23 MM_OVERRIDE	100 MIL_OVERRIDE	VERRIDE	VERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
			PPDDR_MEM	=PP1V5_S3_MEM_A 603 31A5 3107
			PPDDR_MEM	=PP1V5_S3_MEM_B 603 32A5 3207
			SWITCHNODE	IMVP6_PHASE1 7104 71A6
			SWITCHNODE	IMVP6_PHASE2 71C4 71A4
			SWITCHNODE	IMVP6_PHASE3 72C6 72A7
			SWITCHNODE	1V8_SW 88C5
			SWITCHNODE	1V85S5_SW 79C5
			SWITCHNODE	P1V85S0_PHASE 76C6
			SWITCHNODE	3V3S5_SW 76C3
			SWITCHNODE	5VS3_SW 73C5
			SWITCHNODE	MCPCORES0_PHASE 74C5
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP1_DN6 95A8 9506 95
		THERM_DIFF	THERMAL	SNS_T_DN1_DP6 95A8 9506 95
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP2_DN3 95A8 95C6 95
		THERM_DIFF	THERMAL	SNS_T_DN2_DP3 95A8 95C6 95
	THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P 10C6 95D4
		THERM_DIFF	THERMAL	CPU_THERMD_N 10C6 95D4
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_T_DP4_DN5 95A8 9586 95
		THERM_DIFF	THERMAL	SNS_T_DN4_DP5 95A8 9586 95
	THERM_DIFF	THERM_DIFF	THERMAL	MCP_THMDIODE_P 21C3 95C4
		THERM_DIFF	THERMAL	MCP_THMDIODE_N 21C3 95C4
	THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_D2_P 95B3
		THERM_DIFF	THERMAL	MCPTHMSNS_D2_N 95B3
	THERM_DIFF	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P 93C4
		THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N 93C4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S0_P 93B3 93B4
		THERM_DIFF	THERMAL	SENSE_12V_S0_N 93B3 93B4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE_12V_S5_P 93B3 93C4
		THERM_DIFF	THERMAL	SENSE_12V_S5_N 93B3 93C4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE_1V5_S0_P 94D6
		THERM_DIFF	THERMAL	SENSE_1V5_S0_N 94D6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_LCD_P 95C7
		THERM_DIFF	THERMAL	SNS_LCD_N 95C7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_ODD_P 95D7
		THERM_DIFF	THERMAL	SNS_ODD_N 95D7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_CPU_H_P 95B7
		THERM_DIFF	THERMAL	SNS_CPU_H_N 95B7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_HDD_P 95D6
		THERM_DIFF	THERMAL	SNS_HDD_N 95D6
	THERM_DIFF	THERM_DIFF	THERMAL	HDD_O0B_TEMP_FILT 95D6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_AMB_P 95C6
		THERM_DIFF	THERMAL	SNS_AMB_N 95C6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS_MXM_P 95B6
		THERM_DIFF	THERMAL	SNS_MXM_N 95B6
	THERM_DIFF	THERM_DIFF	THERMAL	MCPTHMSNS_FILT_P 95B4
		THERM_DIFF	THERMAL	MCPTHMSNS_FILT_N 95B4

K50/K51 SPECIFIC CONSTRAINTS

SYNC_MASTER=AARON	SYNC_DATE=05/20/2008
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